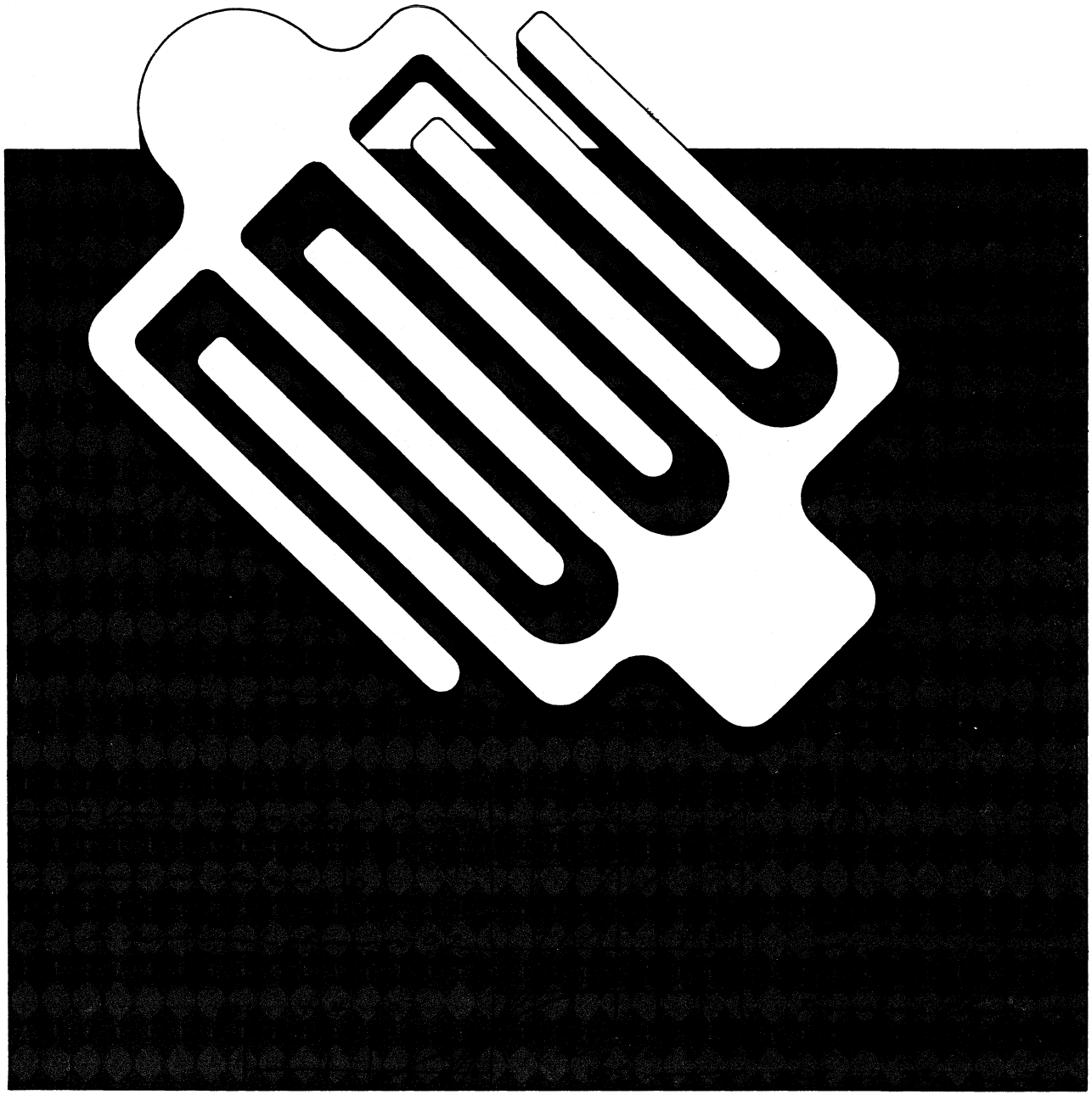
Intersil

Field Effect Transistors
Dual Bipolar Transistors

Discrete Semiconductor Guide



INTRODUCTION

THE COMPANY

Since its founding on July 26, 1967 INTERSIL, INC., has assumed a leading role in semiconductor research and manufacturing. The INTERSIL team is made up of some of the world's most experienced talents in semiconductor development and processing. Its key members represent the broadest cross section of scientific, marketing, engineering, and production background in the semiconductor field. Each team member is a specialist in his own field, with a deep insight into the related team activities. The technical know-how, inventiveness, and production experience represented by these specialists combine to offer INTERSIL's customers the most reliable, advanced state-of-the-art semiconductor devices available on today's market.

THE PRODUCTS

INTERSIL produces a broad line of discrete semiconductor devices which includes single and monolithic dual Field Effect Transistors of both the junction and MOS type, and high-performance monolithic dual NPN and PNP bipolar transistors.

QUALITY

The INTERSIL high reliability facility at Cupertino, California has been certified by the Defense Electronics Supply Center (DESC) as meeting the requirements of MIL-S-19500.

All devices are 100% visually pre-cap inspected to MIL-STD-750, method 2072. The guaranteed quality assurance level is to a 5% LTPD MIL-S-19500. In addition, all wafer lots are sample inspected using a Scanning Electronic Microscope (SEM) at a magnification of 6000X minimum. Electrical parameters are guaranteed to a 5% LTPD.

APPLICATIONS

As a maker of a broad line of sophisticated high-performance discrete devices, INTERSIL recognizes its responsibility to provide technical applications assistance. INTERSIL's commitment to the technical support of the user community goes well beyond a thorough understanding of device characteristics and into an ability to solve problems at the circuit design level.

HOW TO USE THIS PRODUCT GUIDE

Alpha-numeric Listing ... use this index to find a device for which you have a number. (Page 3.)

Cross-reference List ... use this index to cross reference an industry standard device type to an INTERSIL device type. (Page 6.)

Product by Category Listing ... use this index to select a device type by the appropriate application. (Page 13.)

CONTENTS

ALPHA-NUMERIC LISTING BY DEVICE TYPE

ALPHA-NUMERIC LISTING BY DEVICE TYPE

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CROSS REFERENCE LIST

USE OF CROSS - REFERENCE LIST

PREFERRED PARTS

If the Intersil number is the same as the industry number, Intersil supplies this part as a preferred part. This means that it is considered a standard stock item. A description of each preferred part is provided within this catalog.

For example:	Industry	Intersil	Category
	2N4391	2N4391	A

INDUSTRY NUMBER IS ASTERISKED

Intersil can provide the industry number, but recommends the Intersil preferred number for optimum pricing and availability. If the Intersil preferred part is selected, the data sheet must be consulted since the device may not always be identical.

For example:	Industry		Intersil	Category
	2N2639	*	IT120	G

INDUSTRY AND INTERSIL NUMBERS ARE DIFFERENT AND THERE IS NO ASTERISK

If the Intersil number is different from the industry number, and if the industry number is not asterisked, Intersil does not make the industry number and therefore recommends the Intersil preferred part only. Consult the Intersil data sheet for specification differences.

For example:	Industry	Intersil	Category
	2N3084	2N4339	C

NON-STANDARD PACKAGE ORDERING INFORMATION

If you want 2N4091 in a TO-18 package, order 2N4091.

If you want 2N4091 in a TO-92 package, order 2N4091/TO-92.

If you want 2N4091 in wafer form, order 2N4091/W.

If you want 2N4091 in chip form, order 2N4091/D.

CROSS REFERENCE LIST

Industry		Preferred Intersil	Cat.
2N2386		2N2608	D
2N2386A		2N2608	D
2N2453		2N2453	G
2N2453A		2N2453A	G
2N2497		2N2608	D
2N2498		2N2608	D
2N2499		2N2609	D
2N2500		2N2608	D
2N2606		2N2606	D
2N2607		2N2607	D
2N2608		2N2608	D
2N2609		2N2609	D
2N2639	*	IT120	G
2N2640	*	IT122	G
2N2641	*	IT122	G
2N2642	*	IT120	G
2N2643	*	IT122	G
2N2644	*	IT122	G
2N2720	*	IT120	G
2N2721	*	IT122	G
2N2722	*	IT120	G
2N2841	*	2N2607	D
2N2842	*	2N2607	D
2N2843	*	2N2607	D
2N2844	*	2N2607	D
2N2903	*	IT122	G
2N2903A	*	IT120	G
2N2913	*	IT122	G
2N2914	*	IT122	G
2N2915	*	IT120	G
2N2915A	*	IT120	G
2N2916	*	IT120	G
2N2916A	*	IT120	G
2N2917	*	IT122	G
2N2918	*	IT122	G
2N2919	*	IT120	G
2N2919A	*	IT120	G
2N2920	*	IT120	G
2N2920A	*	IT120	G
2N2936	*	IT120	G
2N2937	*	IT120	G
2N2972		IT122	G
2N2973		IT122	G
2N2974		IT120	G
2N2975		IT120	G
2N2976		IT120	G
2N2977		IT120	G
2N2978		IT120	G
2N2979		IT120	G
2N3066	*	2N4220	C
2N3067	*	2N3686	C
2N3068	*	2N3687	C
2N3069	*	2N4341	C
2N3070	*	2N4339	C
2N3071	*	2N4338	C
2N3084		2N4339	C
2N3085	*	2N4339	C
2N3086		2N4339	C
2N3087	*	2N4339	C
2N3088		2N4339	C
2N3088A		2N4339	C
2N3089	*	2N4339	C
2N3089A	*	2N4339	C
2N3277		2N2606	D
2N3278		2N2607	D
2N3328	*	2N5265	D
2N3329		2N3329	D
2N3330		2N3330	D
2N3331		2N3331	D
2N3332	*	2N3330	D
2N3347	*	IT137	G
2N3348	*	IT138	G
2N3349	*	IT139	G
2N3350	*	IT137	G
2N3351	*	IT138	G
2N3352	*	IT139	G
2N3365	*	2N4220	C
2N3366	*	2N3686	C
2N3367	*	2N3687	C
2N3368	*	2N4341	C
2N3369	*	2N4339	C
2N3370	*	2N4338	C
2N3376	*	2N3330	D
2N3378	*	2N3330	D
2N3380	*	2N3331	D
2N3382	*	2N3994	A
2N3384	*	2N3993	D
2N3386	*	2N3993	D
2N3436	*	2N4341	D
2N3437	*	2N4340	C
2N3438	*	2N4338	C
2N3452	*	2N4220	C
2N3453	*	2N3686	C
2N3454	*	2N3687	C
2N3455	*	2N3686	C
2N3456	*	2N3686	C
2N3457	*	2N3687	C
2N3458	*	2N4341	C
2N3459	*	2N4339	C
2N3460	*	2N4338	C
2N3574	*	2N5265	D
2N3575	*	2N5265	D
2N3578	*	2N2608	D
2N3608	*	3N172	B
2N3680	*	IT120	G
2N3684		2N3684	C
2N3684A	*	2N3684	C
2N3685		2N3685	C
2N3685A	*	2N3685	C
2N3686		2N3686	C
2N3686A	*	2N3686	C
2N3687		2N3687	C
2N3687A	*	2N3687	C
2N3800		IT132	G
2N3801		IT132	G
2N3802		IT132	G
2N3803		IT132	G
2N3804		IT130	G
2N3804A		IT130A	G
2N3805		IT130	G
2N3805A		IT130A	G
2N3806	*	IT132	G
2N3807	*	IT132	G
2N3808	*	IT132	G
2N3809	*	IT132	G
2N3810	*	IT130	G
2N3810A	*	IT130A	G
2N3811	*	IT130	G
2N3811A	*	IT130A	G
2N3821		2N3821	C
2N3822		2N3822	C
2N3823	*	2N4416	C
2N3824	*	2N5397	C
2N3907	*	IT120	G
2N3908	*	IT120	G
2N3909	*	2N3331	D
2N3909A	*	2N3331	D
2N3921	*	SU2365	E
2N3922	*	SU2367	E
2N3954		2N3954	E
2N3954A		2N3954A	E
2N3955		2N3955	E
2N3955A		2N3955A	E
2N3956		2N3956	E
2N3957		2N3957	E
2N3958		2N3958	E
2N3966	*	2N4416	E
2N3967	*	2N4221	C
2N3967A	*	2N4221	C
2N3968	*	2N3685	C
2N3968A	*	2N3685	C
2N3969	*	2N3686	C
2N3969A	*	2N3686	C
2N3970	*	2N4391	A
2N3971	*	2N4392	A
2N3972	*	2N4393	A
2N3993		2N3993	A
2N3993A	*	2N3993	A
2N3994		2N3994	A
2N3994A	*	2N3994	A
2N4017		IT139	G
2N4018		IT139	G
2N4019		IT139	G
2N4020		IT139	G
2N4021		IT139	G
2N4022		IT139	G
2N4023		IT137	G
2N4024		IT137	G
2N4025		IT137	G
2N4044		2N4044	G
2N4045		2N4045	G
2N4065	*	3N163	B
2N4066	*	3N166	F
2N4067	*	3N166	F
2N4082	*	SU2366	E
2N4083	*	2N2368	E
2N4084		2N3954	E
2N4085		2N3955	E
†2N4091		†2N4091	A
†2N4092		†2N4092	A
†2N4093		†2N4093	A
2N4100		2N4100	G
2N4117		2N4117	C

† JTX version available.

CROSS REFERENCE LIST

Industry		Preferred Intersil	Cat.
2N4117A		2N4117A	C
2N4118		2N4118	C
2N4118A		2N4118A	C
2N4119		2N4119	C
2N4119A		2N4119A	C
2N4120	*	3N163	B
2N4139	*	2N3822	C
2N4220		2N4220	C
2N4220A	*	2N4220	C
2N4221		2N4221	C
2N4221A	*	2N4221	C
2N4222		2N4222	C
2N4222A	*	2N4222	C
2N4223		2N4223	C
2N4224		2N4224	C
2N4267	*	3N163	B
2N4268	*	3N160	B
2N4302		2N5457	C
2N4303		2N5459	C
2N4304		2N5458	C
2N4338		2N4338	C
2N4339		2N4339	C
2N4340		2N4340	C
2N4341		2N4341	C
2N4342		2N5461	D
2N4343		2N5462	D
2N4351		2N4351	B
2N4352		3N163	B
2N4353	*	3N172	B
2N4360		2N5460	D
2N4381		2N2609	D
2N4382		2N5115	A
2N4391		2N4391	A
2N4392		2N4392	A
2N4393		2N4393	A
2N4416		2N4416	C
2N4416A	*	2N4416	C
2N4417		2N4416	C
2N4445		2N5432	A
2N4446		2N5434	A
2N4447		2N5432	A
2N4448		2N5434	A
2N4856		2N4856	A
2N4856A	*	2N4856	A
2N4857		2N4857	A
2N4857A	*	2N4857	A
2N4858		2N4858	A
2N4858A	*	2N4858	A
2N4859		2N4859	A
2N4859A	*	2N4859	A
2N4860		2N4860	A
2N4860A	*	2N4860	A
2N4861		2N4861	A
2N4861A	*	2N4861	A
2N4867		2N4867	C
2N4867A		2N4867A	C
2N4868		2N4868	C
2N4868A		2N4868A	C
2N4869		2N4869	C
2N4869A		2N4869A	C
2N4878		2N4878	G
2N4879		2N4879	G
2N4880		2N4880	G
2N4955		IT132	G
2N4956		IT132	G
2N4977	*	2N5433	A
2N4978	*	2N5433	A
2N4979	*	2N4859	A
2N5018	*	2N5114	A
2N5019	*	2N5115	A
2N5020	*	2N2607	D
2N5021	*	2N2608	D
2N5033		2N5460	D
2N5045	*	2N5453	E
2N5046	*	2N5454	E
2N5047	*	2N5454	E
2N5078	*	2N5397	C
2N5103	*	2N4221	C
2N5104	*	2N4416	C
2N5105	*	2N4416	C
†2N5114		†2N5114	A
†2N5115		†2N5115	A
†2N5116		†2N5116	A
2N5117		2N5117	G
2N5118		2N5118	G
2N5119		2N5119	G
2N5163		2N3822	C
2N5196		2N5196	E
2N5197		2N5197	E
2N5198		2N5198	E
2N5199		2N5199	E
2N5245		2N4416	C
2N5246		2N5484	C
2N5247		2N5486	C
2N5248		2N5485	C
2N5254		IT132	G
2N5255		IT132	G
2N5256		IT130	G
2N5265		2N5265	D
2N5266		2N5266	D
2N5267		2N5267	D
2N5268		2N5268	D
2N5269		2N5269	D
2N5270		2N5270	D
2N5277		2N4341	C
2N5278		2N4341	C
2N5358	*	2N3686	C
2N5359	*	2N3686	C
2N5360	*	2N3685	C
2N5361	*	2N3684	C
2N5362	*	2N3684	C
2N5363	*	2N4416	C
2N5364	*	2N4224	C
2N5391		2N4867A	C
2N5392		2N4868A	C
2N5393		2N4869A	C
2N5394		2N4869A	C
2N5395		2N4869A	C
2N5397		2N5397	C
2N5398	*	2N5397	C
2N5432		2N5432	A
2N5433		2N5433	A
2N5434		2N5434	A
2N5452		2N5452	E
2N5453		2N5453	E
2N5454		2N5454	E
2N5457		2N5457	C
2N5458		2N5458	C
2N5459		2N5459	C
2N5460		2N5460	D
2N5461		2N5461	D
2N5462		2N5462	D
2N5463		2N5463	D
2N5464		2N5464	D
2N5465		2N5465	D
2N5471	*	2N5265	D
2N5472	*	2N5265	D
2N5473	*	2N5265	D
2N5474	*	2N5265	D
2N5475	*	2N5265	D
2N5476	*	2N5266	D
2N5484		2N5484	C
2N5485		2N5485	C
2N5486		2N5486	C
2N5515		2N5515	E
2N5516		2N5516	E
2N5517		2N5517	E
2N5518		2N5518	E
2N5519		2N5519	E
2N5520		2N5520	E
2N5521		2N5521	E
2N5522		2N5522	E
2N5523		2N5523	E
2N5524		2N5524	E
2N5545	*	2N3954	E
2N5546	*	2N3955A	E
2N5547	*	2N3955	E
2N5549		2N4392	A
2N5555		2N5555	A
2N5556	*	2N3685	C
2N5557	*	2N3684	C
2N5558	*	2N3684	C
2N5561	*	SU2365	E
2N5562	*	SU2366	E
2N5563	*	SU2368	E
2N5638		2N5638	A
2N5639		2N5639	A
2N5640		2N5640	A
2N5647		2N4117A	C
2N5648		2N4117A	C
2N5649		2N4117A	C
2N5653	*	2N5638	A
2N5654	*	2N5639	A
2N5668	*	2N5484	C
2N5669	*	2N5485	C
2N5670	*	2N5486	C
2N5902		2N5902	E
2N5903		2N5903	E
2N5904		2N5904	E
2N5905		2N5905	E
2N5906		2N5906	E
2N5907		2N5907	E
2N5908		2N5908	E

† JTX version available.

CROSS REFERENCE LIST

Industry		Preferred Intersil	Cat.
2N5909		2N5909	E
2N5911		2N5911	E
2N5912		2N5912	E
2N5949		2N4416	C
2N5950		2N4416	C
2N5951		2N4416	C
2N5952		2N5485	C
2N5953		2N4221	C
2N6451		2N4868A	C
2N6452		2N4869A	C
2N6453		2N4868A	C
2N6454		2N4869A	C
2N6483		2N6483	E
2N6484		2N6484	E
2N6485		2N6485	E
3N145	*	3N163	B
3N146	*	3N163	B
3N147		3N147	F
3N148		3N148	F
3N149	*	3N160	B
3N150	*	3N163	B
3N151	*	3N163	B
3N155		3N163	B
3N155A		3N163	B
3N156		3N163	B
3N156A		3N163	B
3N157		3N163	B
3N157A		3N163	B
3N158		3N163	B
3N158A		3N163	B
3N160		3N160	B
3N161		3N161	B
3N163		3N163	B
3N164	*	3N163	B
3N165		3N165	F
3N166		3N166	F
3N167		3N161	B
3N168		3N161	B
3N169		3N169	B
3N170		3N170	B
3N171		3N171	B
3N172		3N172	B
3N173	*	3N172	B
3N174	*	3N163	B
3N175	*	3N169	B
3N176	*	3N170	B
3N177	*	3N171	B
3N178	*	3N172	B
3N179	*	3N172	B
3N180	*	3N172	B
3N181		3N161	B
3N182		3N161	B
3N183		3N161	B
3N188		3N188	F
3N189		3N189	F
3N190		3N190	F
3N191		3N191	F
AD810	*	2N4880	G
AD811	*	2N4879	G
AD812	*	2N4878	G
AD813	*	2N4878	G
AD820	*	IT132	G
AD821	*	IT130	G
AD822	*	IT130A	G
AD830		2N5520	E
AD931		2N5521	E
AD832		2N5522	E
AD833		2N5523	E
AD833A		2N5524	E
AD840		2N5520	E
AD841		2N5521	E
AD842		2N5523	E
AD3954		2N3954	E
AD3954A		2N3954A	E
AD3955		2N3955	E
AD3956		2N3956	E
AD3958		2N3958	E
AD5905		2N5905	E
AD5906		2N5906	E
AD5907		2N5907	E
AD5908		2N5908	E
AD5909		2N5909	E
BF348		2N5397	C
C413N		2N5434	A
CM800		2N4091	A
CP643		2N4091	A
CP640		2N5433	A
CP650		2N5432	A
CP651		2N5433	A
CP652		2N5433	A
CP653		2N5433	A
DU4340		2N3958	E
E100		2N5458	C
E101		2N4338	C
E102		2N5457	C
E103		2N5459	C
E105		2N5432	A
E106		2N5433	A
E107		2N5433	A
E108		2N5433	A
E109		2N5433	A
E110		2N5434	A
E111		2N4091	A
E112		2N4092	A
E113		2N4093	A
E114		2N5555	A
E174		2N5114	A
E175		2N5115	A
E176		2N5116	A
E201		2N4338	C
E202		2N4340	C
E203		2N4341	C
E210		2N5397	C
E211		2N5397	C
E212		2N5397	C
E230		2N4340	C
E231		2N4341	C
E232		2N4341	C
E270		2N4393	A
E271		2N4392	A
E300		2N5397	C
E304		2N4416	C
E305		2N5484	C
E308		U308	C
E309		U309	C
E310		U310	C
E311		U311	C
E312		U310	C
E400		2N5453	E
E401		2N3955	E
E402		2N3956	E
E413		2N5454	E
E414		2N3956	E
E415		2N3957	E
E420		2N5911	E
E421		2N5912	E
FE0654A		2N5486	C
FE0654B		2N5485	C
FE5245		2N4416	C
FE5246		2N5486	C
FE5247		2N5486	C
FE5457		2N5457	C
FE5458		2N5458	C
FE5459		2N5459	C
FE5484		2N5484	C
FE5485		2N5485	C
FE5486		2N5486	C
FT0654A		2N5486	C
FT0654B		2N5486	C
ID100		ID100	G
ID101		ID101	G
IMF3954	*	2N3954	E
IMF3954A	*	2N3954A	E
IMF3955	*	2N3955	E
IMF3955A	*	2N3955A	E
IMF3956	*	2N3956	E
IMF3957	*	2N3957	E
IMF3958	*	2N3958	E
IMF6485		IMF6485	E
IT108		2N5486	C
IT109		2N5397	C
IT100		IT100	A
IT101		IT101	A
IT120		IT120	G
IT120A		IT120A	G
IT121		IT121	G
IT122		IT122	G
IT124		IT124	G
IT126		IT126	G
IT127		IT127	G
IT128		IT128	G
IT129		IT129	G
IT130		IT130	G
IT130A		IT130A	G
IT131		IT131	G
IT132		IT132	G
IT136		IT136	G
IT137		IT137	G
IT138		IT138	G
IT139		IT139	G
IT400		IT400	A
IT1700		IT1700	B
IT1701	*	3N172	B

CROSS REFERENCE LIST

Industry		Preferred Intersil	Cat.
IT1702	*	3N163	B
IT1750		IT1750	B
IT2700	*	3N165	F
IT2701	*	3N165	F
ITC2972		IT122	G
ITC2973		IT122	G
ITC2974		IT120	G
ITC2975		IT120	G
ITC2976		IT120	G
ITC2977		IT120	G
ITC2978		IT120	G
ITC2979		IT120	G
ITC3347		IT137	G
ITC3348		IT138	G
ITC3349		IT139	G
ITC3350		IT137	G
ITC3351		IT138	G
ITC3352		IT139	G
ITC3800		IT132	G
ITC3802		IT132	G
ITC3804		IT130	G
ITC3806		IT132	G
ITC3807		IT132	G
ITC3808		IT132	G
ITC3809		IT132	G
ITC3810		IT130	G
ITC3811		IT130	G
ITC4017		IT139	G
ITC4018		IT139	G
ITC4019		IT139	G
ITC4020		IT139	G
ITC4021		IT139	G
ITC4022		IT139	G
ITC4023		IT137	G
ITC4024		IT137	G
ITC4025		IT137	G
ITE2453		IT120	G
ITE2639		IT120	G
ITE2640		IT122	G
ITE2641		IT122	G
ITE2642		IT120	G
ITE2643		IT122	G
ITE2644		IT122	G
ITE2720		IT120	G
ITE2721		IT122	G
ITE2722		IT120	G
ITE2903		IT122	G
ITE2913		IT122	G
ITE2914		IT122	G
ITE2915		IT120	G
ITE2916		IT120	G
ITE2917		IT122	G
ITE2918		IT122	G
ITE2919		IT120	G
ITE2920		IT120	G
ITE2936		IT120	G
ITE2937		IT120	G
ITE2972		IT122	G
ITE2973		IT122	G
ITE2974		IT120	G
ITE2975		IT120	G
ITE2976		IT120	G
ITE2977		IT120	G
ITE2978		IT120	G
ITE2979		IT120	G
ITE3066		2N3685	C
ITE3067		2N3686	C
ITE3068		2N3687	C
ITE3347		IT137	G
ITE3348		IT138	G
ITE3349		IT139	G
ITE3350		IT137	G
ITE3351		IT138	G
ITE3352		IT139	G
ITE3680		IT120	G
ITE3800		IT132	G
ITE3802		IT132	G
ITE3804		IT130	G
ITE3806		IT132	G
ITE3807		IT132	G
ITE3808		IT132	G
ITE3809		IT132	G
ITE3810		IT130	G
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ITE3907		IT120	G
ITE3908		IT120	G
ITE4017		IT139	G
ITE4018		IT139	G
ITE4019		IT139	G
ITE4020		IT139	G
ITE4021		IT139	G
ITE4022		IT139	G
ITE4023		IT137	G
ITE4024		IT137	G
ITE4025		IT137	G
ITE4117		2N4117	C
ITE4118		2N4118	C
ITE4119		2N4119	C
ITE4338		2N4338	C
ITE4339		2N4339	C
ITE4340		2N4340	C
ITE4341		2N4341	C
ITE4391		2N4391	A
ITE4392		2N4392	A
ITE4393		2N4393	A
ITE4416		2N4416	C
ITE4867		2N4867	C
ITE4868		2N4868	C
ITE4869		2N4869	C
KE3684		2N3684	C
KE3685		2N3685	C
KE3686		2N3686	C
KE3687		2N3687	C
KE3823		2N4416	C
KE3970		2N4391	A
KE3971		2N4392	A
KE3972		2N4393	A
KE4091		2N4091	A
KE4092		2N4092	A
KE4093		2N4093	A
KE4220		2N4220	C
KE4221		2N4221	C
KE4222		2N4222	C
KE4223		2N4223	C
KE4224		2N4224	C
KE4391		2N4391	A
KE4392		2N4392	A
KE4393		2N4393	A
KE4416		2N4416	C
KE4856		2N4091	A
KE4857		2N4092	A
KE4858		2N4093	A
KE4859		2N4859	A
KE4860		2N4860	A
KE4861		2N4861	A
KE5103		2N4221	C
KE5104		2N4416	C
KE5105		2N4416	C
M103		3N161	B
M104	*	3N172	B
M106		3N189	F
M107		3N189	F
M108		3N191	F
M113		3N161	B
M114		3N161	B
M116		M116	B
M117		2N4351	B
M119		3N161	B
M511		3N172	B
M511A		3N172	B
M517		3N161	B
MEM511	*	3N172	B
MEM511C	*	3N172	B
MEM517	*	3N172	B
MEM517A	*	3N172	B
MEM517B	*	3N172	B
MEM517C	*	3N172	B
MEM520	*	3N163	B
MEM520C	*	3N163	B
MEM550	*	3N189	F
MEM550C	*	3N189	F
MEM551	*	3N190	F
MEM551C	*	3N190	F
MEM556		3N172	B
MEM556C		3N172	B
MEM560		3N161	B
MEM560C		3N161	B
MEM562		2N4351	B
MEM562C		2N4351	B
MEM563		2N4351	B
MEM563C		2N4351	B
MEM806		3N163	B
MEM806A		3N163	B
MEM807		3N172	B
MEM807A		3N172	B
MFE2000	*	2N4416	C
MFE2001	*	2N4416	C
MFE2004	*	2N4861	A
MFE2005	*	2N4860	A
MFE2006	*	2N4859	A
MFE2007	*	2N4860	A
MFE2008	*	2N4859	A
MFE2009	*	2N4859	A

CROSS REFERENCE LIST

Industry		Preferred Intersil	Cat.	Industry		Preferred Intersil	Cat.	Industry		Preferred Intersil	Cat.
MFE2010	*	2N4859	A	NF5459		2N5459	C	TN4119		2N4119	C
MFE2011	*	2N5433	A	NF5485		2N5485	C	TN4119A		2N4119A	C
MFE2012	*	2N5433	A	NF5486		2N5486	C	TN4338		2N4338	C
MFE2093	*	2N4338	C	NF5555		2N5397	C	TN4339		2N4339	C
MFE2094	*	2N4339	C	NF5638		2N5638	A	TN4340		2N4340	C
MFE2095	*	2N4340	C	NF5639		2N5639	A	TN4341		2N4341	C
MFE2133		2N4861	A	NF5640		2N5640	A	TP5114		2N5114	A
MFE3002		3N169	B	NF5653		2N4860	A	TP5115		2N5115	A
MFE3003		3N163	B	NF5654		2N4861	A	TP5116		2N5116	A
MFE3020	*	3N166	F	P1086E		2N5115	A	U110	*	2N2606	D
MFE3021	*	3N166	F	P1087E		2N5115	A	U112	*	2N2608	D
MFE4007	*	2N3686	C	PF510	*	2N5115	A	U133	*	2N2607	D
MFE4008	*	2N3686	C	PF511	*	2N5115	A	U146	*	2N2606	D
MFE4009	*	2N3685	C	SU2098	*	2N5197	E	U147	*	2N2607	D
MFE4010	*	2N3684	C	SU2098A	*	2N5197	E	U148	*	2N2608	D
MFE4012		2N4416	C	SU2098B	*	2N5196	E	U149	*	2N2608	D
MMT3823		2N4416	C	SU2099	*	2N5198	E	U168	*	2N2608	D
MPF102	*	2N5486	C	SU2099A	*	2N5198	E	U182	*	2N4091	A
MPF103		2N5457	C	SU2365		SU2365	E	U183	*	2N3684	C
MPF104		2N5458	C	SU2365A		SU2365A	E	U184	*	2N4416	C
MPF105		2N5459	C	SU2366		SU2366	E	U197	*	2N3687	C
MPF108	*	2N5486	C	SU2366A		SU2366A	E	U198	*	2N3655	C
MPF109	*	2N5484	C	SU2367		SU2367	E	U199	*	2N3684	C
MPF111	*	2N5458	C	SU2367A		SU2367A	E	U200	*	2N4861	A
MPF112	*	2N5458	C	SU2368		SU2368	E	U201	*	2N4860	A
MPF161	*	2N5462	D	SU2368A		SU2368A	E	U202	*	2N4859	A
MPF256		2N5398	C	SU2369		SU2369	E	U231	*	2N3954	E
MPF820	*	U310	C	SU2369A		SU2369A	E	U232	*	2N3955	E
MPF970		2N5114	A	TD5902		2N5902	E	U233	*	2N3956	E
MPF971		2N5115	A	TD5902A		2N5902	E	U234	*	2N3957	E
MPF4391		2N4391	A	TD5903		2N5903	E	U235	*	2N3958	E
MPF4392		2N4392	A	TD5903A		2N5903	E	U240	*	2N5432	A
MPF4393		2N4393	A	TD5904		2N5904	E	U241	*	2N5433	A
NF500	*	2N4224	C	TD5904A		2N5904	E	U242	*	2N5433	A
NF501	*	2N4224	C	TD5905		2N5905	E	U243	*	2N5433	A
MF510	*	2N4860	A	TD5905A		2N5905	E	U244		2N5433	A
NF511	*	2N4860	A	TD5906		2N5906	E	U248		2N5902	E
NF520	*	2N3684	C	TD5906A		2N5906	E	U248A		2N5906	E
NF521	*	2N3685	C	TD5907		2N5907	E	U249		2N5903	E
NF522	*	2N3686	C	TD5907A		2N5907	E	U249A		2N5907	E
NF523	*	2N3685	C	TD5908		2N5908	E	U250		2N5904	E
MF530	*	2N4341	C	TD5908A		2N5908	E	U250A		2N5908	E
NF531	*	2N4339	C	TD5909		2N5909	E	U251		2N5905	E
NF532	*	2N4341	C	TD5909A		2N5909	E	U251A		2N5909	E
NF533	*	2N4339	C	TD5911		2N5911	E	U252		2N5911	E
NF580		2N5432	A	TD5911A		2N5911	E	U253		2N5912	E
NF581		2N5432	A	TD5912		2N5912	E	U254	*	2N4859	A
NF582		2N5433	A	TD5912A		2N5912	E	U255	*	2N4860	A
NF583		2N5434	A	TIS14	*	2N4340	C	U256	*	2N4861	A
NF584		2N5433	A	TIS41	*	2N4859	A	U257		U257	E
NF585		2N4859	A	TIS73		2N4859	A	U273		2N4117	C
NF4302		2N5457	C	TIS74		2N4860	A	U273A		2N4117A	C
NF4303		2N5459	C	TIS75		2N4861	A	U274		2N4118	C
NF4304		2N5458	C	TIS88		2N4416	C	U274A		2N4118A	C
NF4445		2N5432	A	TIXS33	*	2N4392	A	U275		2N4119	C
NF4446		2N5433	A	TIXS41	*	2N4859	A	U275A		2N4119A	C
NF4447		2N5433	A	TIXS42		2N5639	A	U280		2N5452	E
NF4448		2N5433	A	TN4117		2N4117	C	U281		2N5453	E
NF5163		2N4341	C	TN4117A		2N4117A	C	U282		2N5453	E
NF5457		2N5457	C	TN4118		2N4118	C	U283		2N5453	E
NF5458		2N5458	C	TN4118A		2N4118A	C	U284		2N5454	E

CROSS REFERENCE LIST

Industry		Preferred Intersil	Cat.
U285		2N5454	E
U290		2N5432	A
U291		2N5432	A
U300		IT101	A
U301		2N5115	A
U304		2N5114	A
U305		2N5115	A
U306		2N5116	A
U308		U308	C
U309		U309	C
U310		U310	C
U311		U311	C
U1277	*	2N3654	C
U1278	*	2N3685	C
U1279	*	2N3686	C
U1280	*	2N3654	C
U1281	*	2N4392	A
U1282	*	2N4341	C
U1283	*	2N4340	C
U1284	*	2N4341	C
U1285	*	2N4220	C
U1286	*	2N4341	C
U1287	*	2N4860	A
U1321	*	2N4860	A
U1322	*	2N3822	C
U1323	*	2N3822	C
U1324	*	2N3687	C
U1325	*	2N3686	C
U1714		2N4340	C
U1837E		2N5486	C
U1897E		2N4091	A
U1898E		2N4092	A
U1899E		2N4093	A
U1994E		2N4416	C
U3000	*	2N4341	C
U3001	*	2N4339	C
U3002	*	2N4338	C
U3010	*	2N4341	C
U3011	*	2N4340	C
U3012	*	2N4338	C
UC20		2N3686	C
UC21		2N3687	C
UC100		2N3684	C
UC110		2N3685	C
UC115		2N4340	C
UC130		2N3687	C
UC155		2N5397	C
UC200	*	2N5397	C
UC201	*	2N5397	C
UC210	*	2N3822	C
UC220	*	2N3822	C
UC240	*	2N4340	C
UC241	*	2N4221	C
UC250	*	2N4859	A
UC251	*	2N4861	A
UC400	*	2N3329	D
UC401	*	2N3993	A
UC410	*	2N3330	D
UC420	*	2N3331	D
UC450	*	IT80	A
UC451	*	2N5115	A
UC703	*	2N4220	C
UC704	*	2N4220	C
UC705	*	2N4224	C
UC707	*	2N4860	A
UC714	*	2N4224	C
UC714E		2N5486	C
UC734	*	2N4416	C
UC734E		2N5484	C
UC751	*	2N4340	C
UC752	*	2N4340	C
UC753	*	2N4341	C
UC754	*	2N4340	C
UC755	*	2N4341	C
UC756	*	2N4340	C
UC805	*	2N3331	D
UC807	*	2N4860	A
UC814	*	2N3331	D
UC851	*	2N2608	D
UC853	*	2N2607	D
UC854	*	2N2608	D
UC855	*	2N2609	D
UC1700	*	3N163	B
UC1764	*	3N163	B
UC2130	*	2N5452	E
UC2132	*	2N5453	E
UC2134	*	2N5454	E
UC2136	*	2N5454	E
UC2138	*	2N5454	E
UC2139	*	2N3958	E
UC2147	*	2N3958	E
UC2148	*	2N3958	E
UC2149	*	2N3958	E
UC2766	*	3N166	F

CATEGORY A: SWITCHES—JUNCTION FET

N and P channel junction Field Effect Transistors designed for use in solid-state switching and multiplexing applications. Key parameters of these devices are: $r_{ds(on)}$, $I_{d(off)}$, C_{dgs}, C_{sgs}, $V_{gs(off)}$, BV_{dgs} and BV_{sgs} and, for digital switching applications, $t_{on} + f_{off}$.

Ordering Information: Preferred Part Number	Package	$R_{DS\ (on)}$ max ohm	Vp min/max V	I_{GSS} max pA	BVGSS min V	$I_{D\ (off)}$ max pA	I_{DSS} min/max mA	tap* max nS	C_{ISS} max pf	C_{RSS} max pf
N-channel: Generally requires driver circuit to translate the popular logic levels to voltages required to drive the JFET.										
2N4091	TO-18 TO-92	30	-5.0 -10.0	-200	-40	200	30	65	16	5.0
2N4092	TO-18 TO-92	50	-2.0 -7.0	-200	-40	200	15	95	16	5.0
2N4093	TO-18 TO-92	80	-1.0 -5.0	-200	-40	200	8	140	16	5.0
2N4391	TO-18 TO-92	30	-4.0 -10.0	-100	-40	100	50 150	55	14	3.5
2N4392	TO-18 TO-92	60	-2.0 -5.0	-100	-40	100	25 75	75	14	3.5
2N4393	TO-18 TO-92	100	-0.5 -3.0	-100	-40	100	5 30	100	14	3.5
2N4859	TO-18 TO-92	25	-4.0 -10.0	-250	-30	250	50	34	18	8.0
2N4860	TO-18 TO-92	40	-2.0 -6.0	-250	-30	250	20 100	60	18	8.0
2N4861	TO-18 TO-92	60	-0.8 -4.0	-250	-30	250	8 80	120	18	8.0
2N5432	TO-52 TO-92	5	-4.0 -10.0	-200	-25	200	150	41	30	15.0
2N5433	TO-52 TO-92	7	-3.0 -9.0	-200	-25	200	100	41	30	15.0
2N5434	TO-52 TO-92	10	-1.0 -4.0	-200	-25	200	30	41	30	15.0
2N5555	TO-92	150	-10.0	-1 nA	-25	10 nA	15	35	5	1.2
2N5638	TO-92	30	-12.0	-1 nA	-30	1 nA	50	24	10	4.0
2N5639	TO-92	60	-8.0	-1 nA	-30	1 nA	25	54	10	4.0
2N5640	TO-92	100	-6.0	-1 nA	-30	1 nA	5	63	10	4.0
P-channel: Can be used to switch into inverting input of op-amps and needs no driver circuit; can be switched directly from TTL logic.										
2N3993	TO-72	150	4.0 9.5	1.2 nA	25	1.2 nA	-10		16	4.5
2N3994	TO-72	300	1.0 5.5	1.2 nA	25	1.2 nA	-2		16	4.5
2N5114	TO-18 TO-92	75	5.0 10.0	500	30	500	-30 -90	37	25	7.0
2N5115	TO-18 TO-92	100	3.0 6.0	500	30	500	-15 -60	68	25	7.0
2N5116	TO-18 TO-92	150	1.0 4.0	500	30	500	-5 -25	102	25	7.0
IT100	TO-18 TO-92	75	2.0 4.5	200	35	100	-10		35	12.0
IT101	TO-18 TO-92	60	4.0 10.0	200	35	100	-20		35	12.0

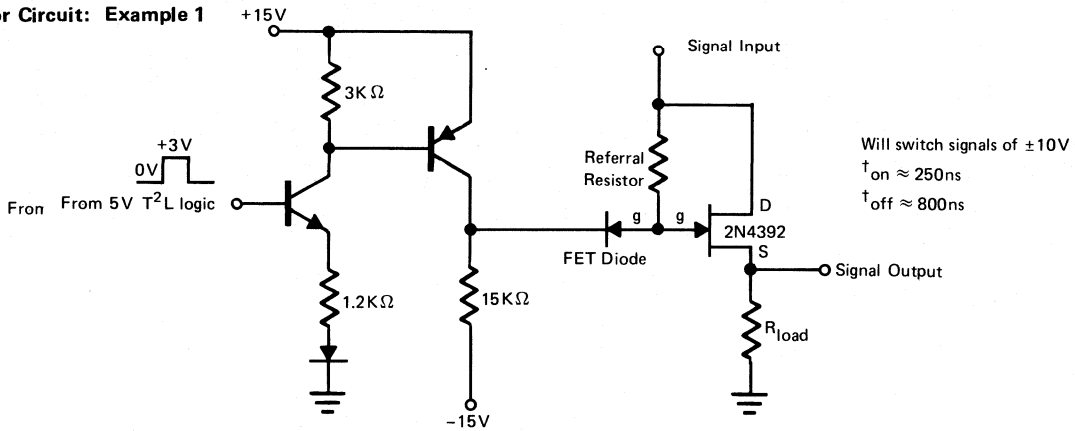
*tap = td (on) + td (off) + tf.

PRODUCT-BY-CATEGORY LISTING: CATEGORY A

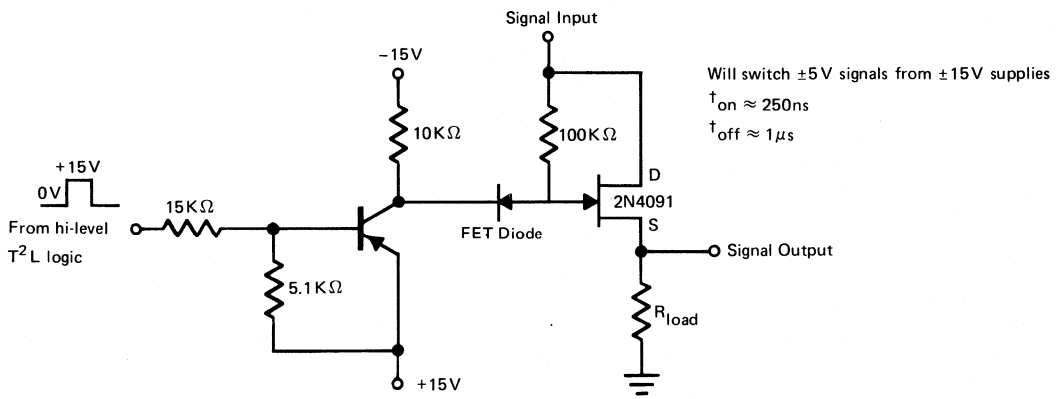
APPLICATION TIPS ON CATEGORY A

These N-channel JFETs are generally used as solid state switches to replace mechanical relays. FETs normally require a driver circuit to translate the TTL logic levels into signal levels high enough to drive the FET.

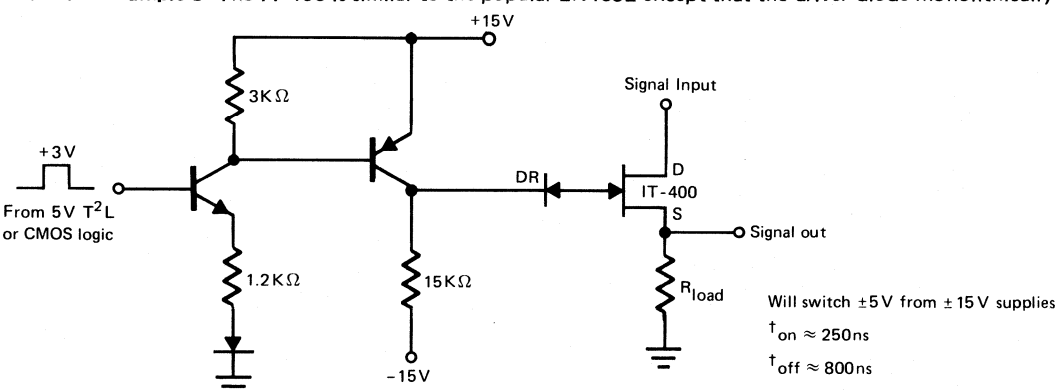
Translator Circuit: Example 1



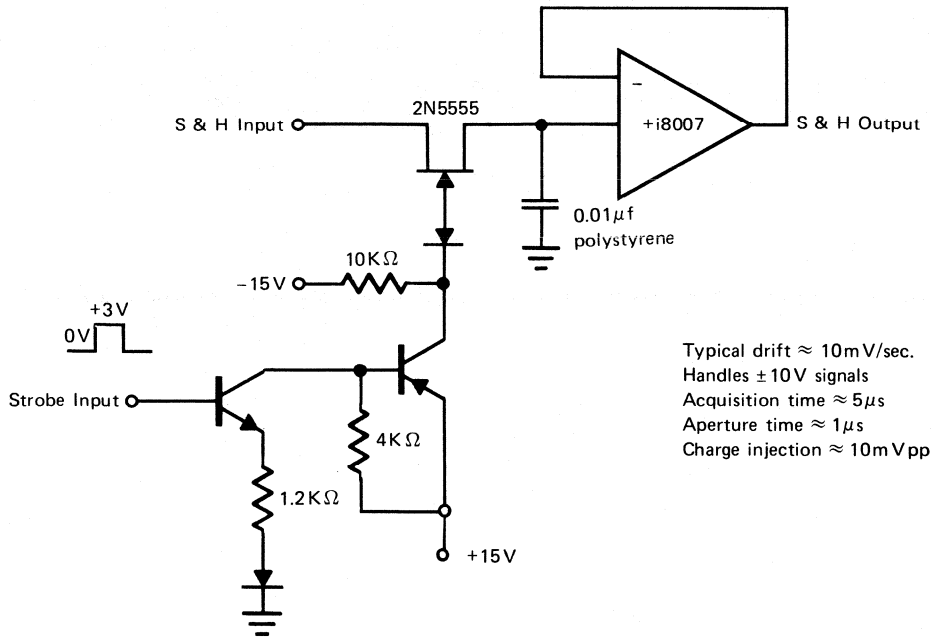
Translator Circuit: Example 2



Translator Circuit: Example 3 The IT-400 is similar to the popular 2N4092 except that the driver diode monolithically is built in.

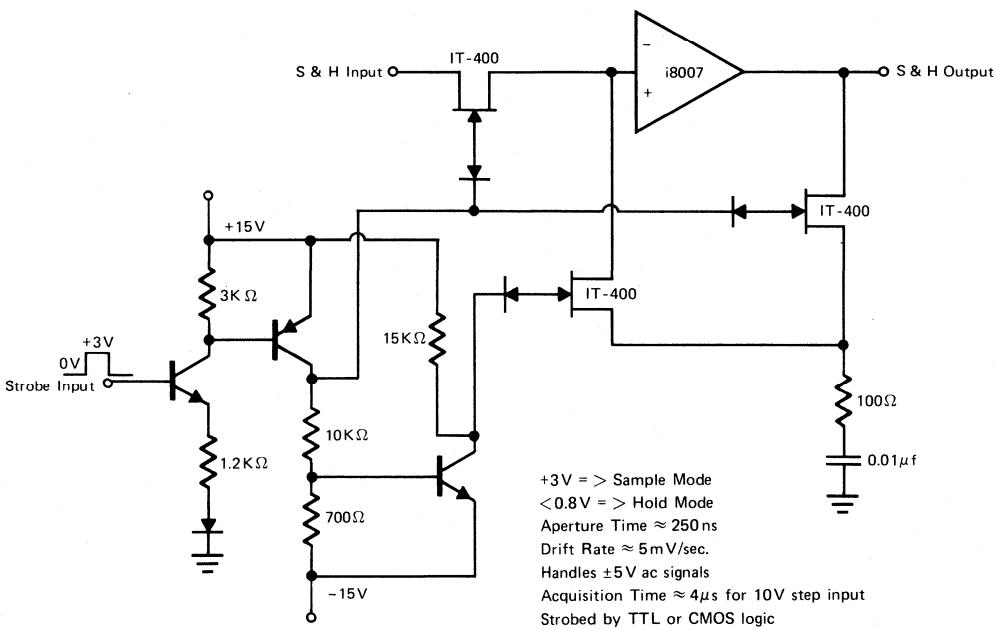


Simple sample and hold circuit using the 2N5555 JFET.



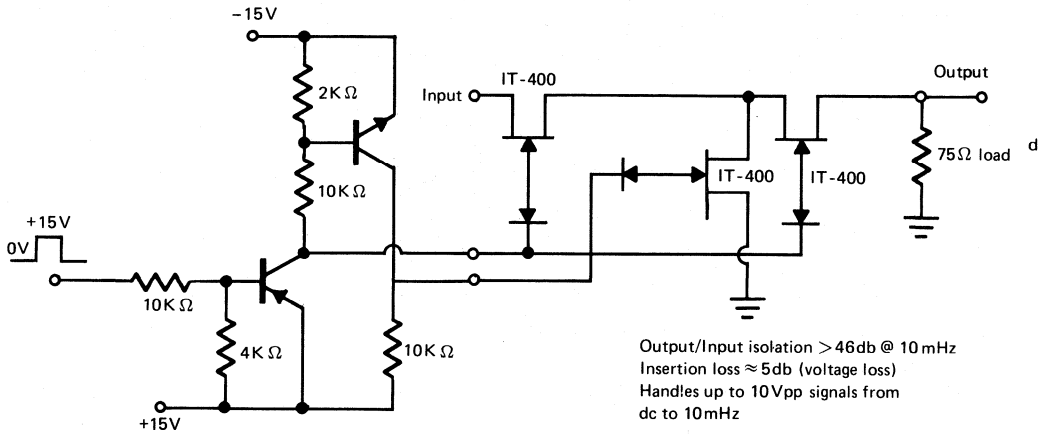
Typical drift ≈ 10mV/sec.
Handles ±10V signals
Acquisition time ≈ 5μs
Aperture time ≈ 1μs
Charge injection ≈ 10mVpp

Switched sample and hold or track and hold circuit, using IT-400 VARAFET.



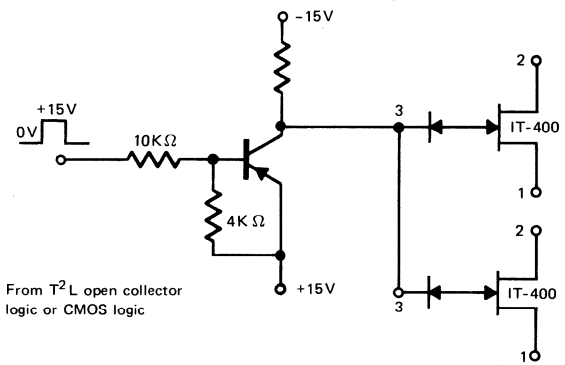
+3V = > Sample Mode
<0.8V = > Hold Mode
Aperture Time ≈ 250ns
Drift Rate ≈ 5mV/sec.
Handles ±5V ac signals
Acquisition Time ≈ 4μs for 10V step input
Strobed by TTL or CMOS logic

Typical applications using the IT-400: Video Switch



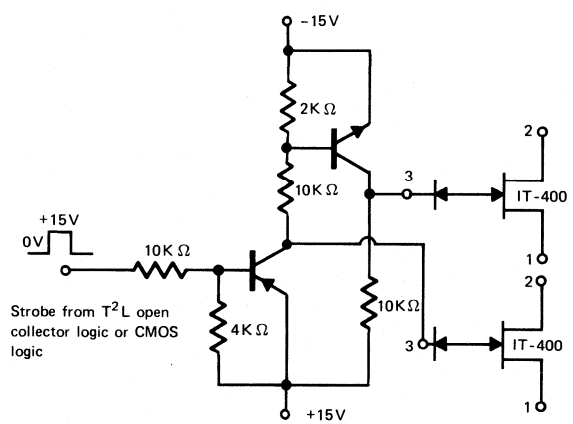
Output/Input isolation >46db @ 10mHz
Insertion loss ≈5db (voltage loss)
Handles up to 10Vpp signals from dc to 10mHz

DPST Switch



Switches are "on" or "off" together to form a double pole configuration

SPDT Switch

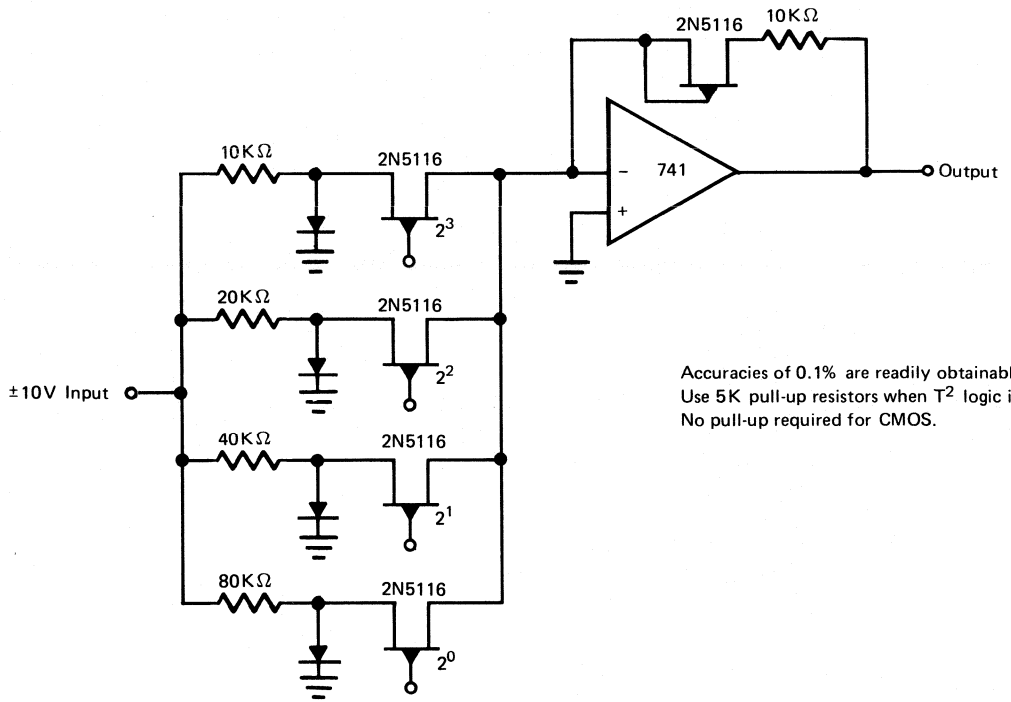


Both switch configurations can handle ±5V ac w/±15V supplies

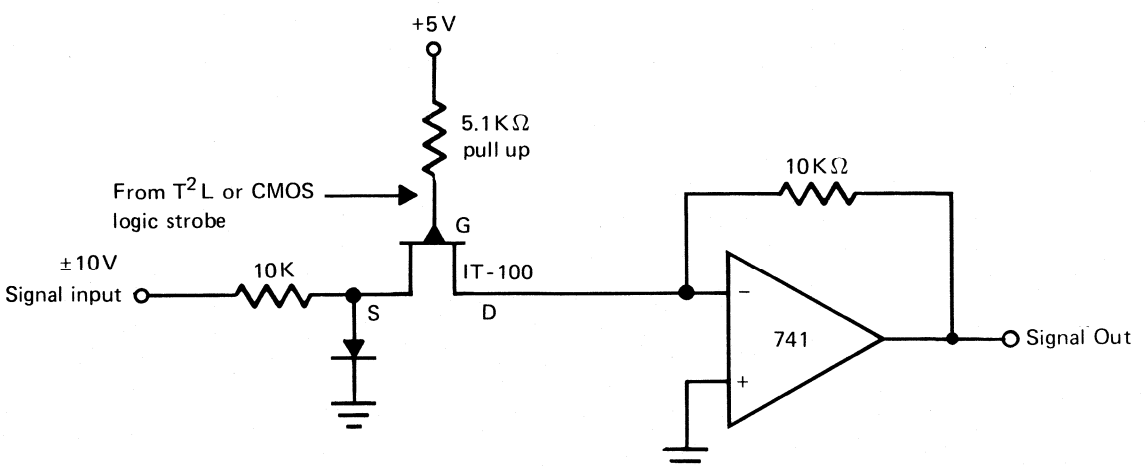
Switches are 180° out of phase. When strobe is high (+15V) lower switch is off and upper switch is on

These P-channel J-FETs are ideal for inverted switching or "virtual gnd" switching. There is no limit as to the signals they can handle. These FETs can be directly driven from TTL or CMOS logic with no translator required.

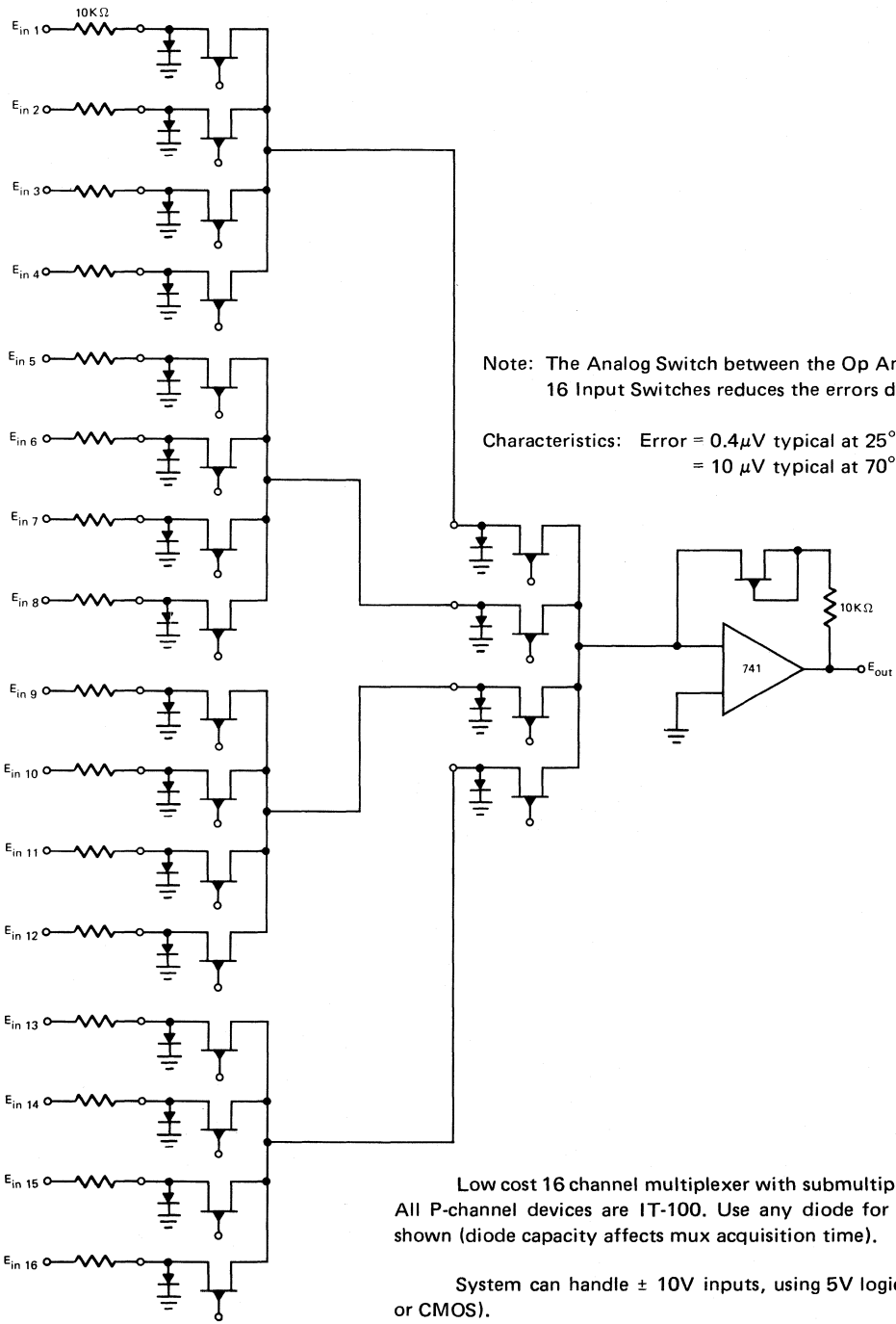
Using 2N5116 as a D to A (Digital to Analog) converter Switching Element.



Accuracies of 0.1% are readily obtainable.
Use 5K pull-up resistors when T^2 logic is used.
No pull-up required for CMOS.



Muxer using IT-100s.



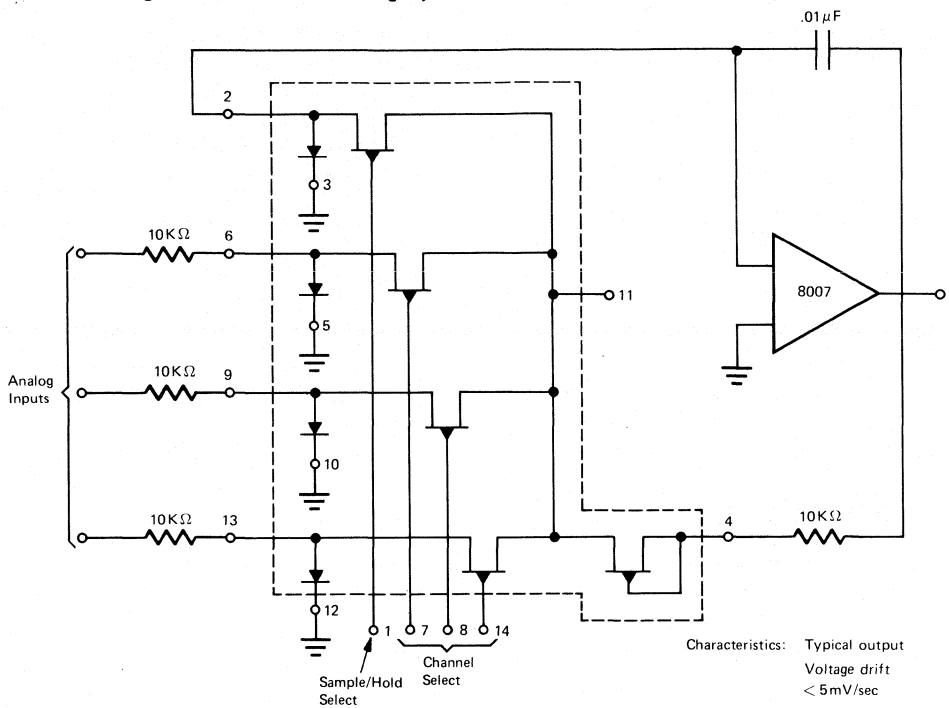
Note: The Analog Switch between the Op Amp and the 16 Input Switches reduces the errors due to leakage.

Characteristics: Error = 0.4μV typical at 25°C
= 10 μV typical at 70°C

Low cost 16 channel multiplexer with submultiplexing. All P-channel devices are IT-100. Use any diode for diodes shown (diode capacity affects mux acquisition time).

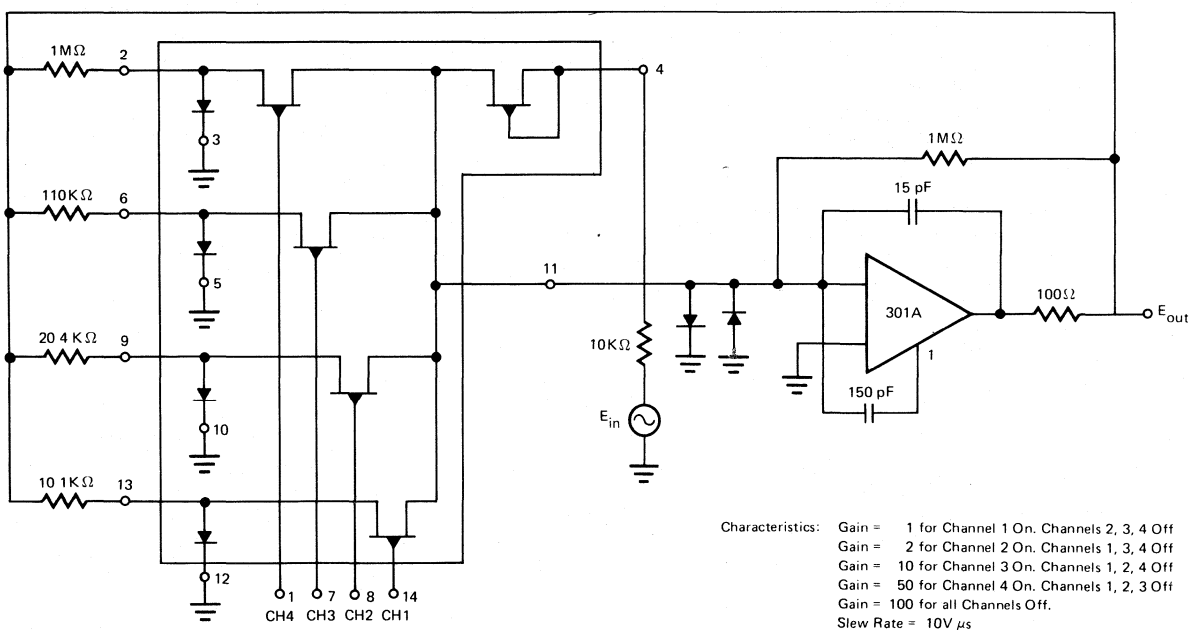
System can handle ± 10V inputs, using 5V logic (T^2L or CMOS).

3 Channel multiplexer with sample and hold (inverting S & H) using the IT-101s. Drive from +12V or +15V logic to handle ± 10V analog inputs.



Characteristics: Typical output Voltage drift < 5mV/sec

Gain ranging circuit using the IT-101s drive from +5V logic to handle ± 10V analog signals



Characteristics:
Gain = 1 for Channel 1 On. Channels 2, 3, 4 Off
Gain = 2 for Channel 2 On. Channels 1, 3, 4 Off
Gain = 10 for Channel 3 On. Channels 1, 2, 4 Off
Gain = 50 for Channel 4 On. Channels 1, 2, 3 Off
Gain = 100 for all Channels Off.
Slew Rate = 10V μs

PRODUCT-BY-CATEGORY LISTING: CATEGORY B

CATEGORY B: SWITCHES AND AMPLIFIERS—MOSFET

N and P channel enhancement mode MOS FETs designed for use in solid-state switching, multiplexing and amplifier applications. Key parameters are I_{gss}, I_{dss}, $V_{gs(th)}$, $V_{ds(on)}$, $r_{ds(on)}$, C_{iss}, $C_{d(sub)}$ and $t_{on} + f_{off}$.

Ordering Information Preferred Part Number	Package	VGS (TH) *VGS (off) min/max V	BVDSS min V	IDSS max pA	IGSS max pA	GFS min μmho	RDS (on) max ohm	ID (on) min mA
P-channel Enhancement: Gen. used where max isolation btwn. signal source and logic drive req'd: sw. "On" resistance varies with signal amplitude								
3N161	TO-72	-1.5 -5.0	-25	-10 nA	-100.0	3500		-40 -120 Diode Protected
3N163	TO-72	-2.0 -5.0	-40	-200	-10.0	2000	250	-5 -30
3N172	TO-72	-2.0 -5.0	-40	-400	-10.0	1500	250	-5 -30 Diode Protected
N-channel Enhancement: Can switch positive signals directly from TTL logic; gen. requires driver or translator circuit to switch bipolar signals								
2N4351	TO-72	1.0 5.0	25	10 nA	10.0	1000	300	3
3N169	TO-72	0.5 1.5	25	10 nA	10.0	1000	200	10
3N170	TO-72	1.0 2.0	25	10 nA	10.0	1000	200	10
3N171	TO-72	1.5 3.0	25	10 nA	10.0	1000	200	10

APPLICATION TIPS ON CATEGORY B

The P-channel, enhancement mode MOSFET, is ideal for multiplexing, crosspoint switching and general switching where low "on" resistance is not a prime requirement. The "on" resistance does vary with signal level so these parts should work into high impedance loads. Generally a driver or translator is required to boost the strobing levels (usually 0V to 5V) up to levels sufficient to enhance the FET (usually ± 15V).

Using the floating body MOSFET structure in analog switching applications.

A typical problem concerned with using MOSFETs in analog switching applications is the change of threshold with varying body to source voltages. The problem is particularly critical when using N-channel devices since these exhibit the greatest variance of circuit threshold (with varying body to source voltages). The origin of the problem can be seen in the circuit below:

In Fig. A. we are switching +10V with a ± 15V power supply (through a driver or translator circuit). The gate is at +15V (corresponds to the enhancement or "on" case) and the body is at -15V. Normally the body of an N-channel MOSFET should be at the most negative potential of the circuit. This gives us a V_{gs} = 5V and a V_{bs} = -25V.

In Fig. B we are switching a signal close to gnd, or a low level signal. For the purpose of making the point, let's say the signal input voltage is 0V. Then we have a V_{gs} = 15V and a V_{bs} = -15V.

In Fig. C the signal input goes to -10V. Then the V_{gs} = 25V and the V_{bs} = -5V.

Now the circuit threshold of an N-channel MOSFET can be described mathematically by V_{gs} (in circuit use) = $V_{th.w/V_{bs}} = 0 + 2.5\sqrt{V_{bs}}$.

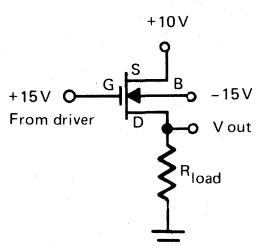


Figure A

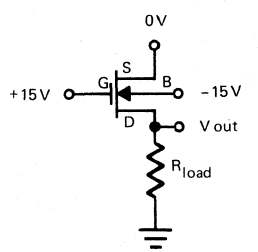


Figure B

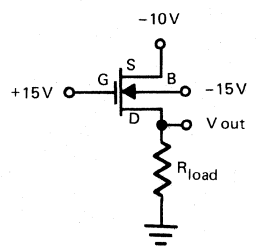


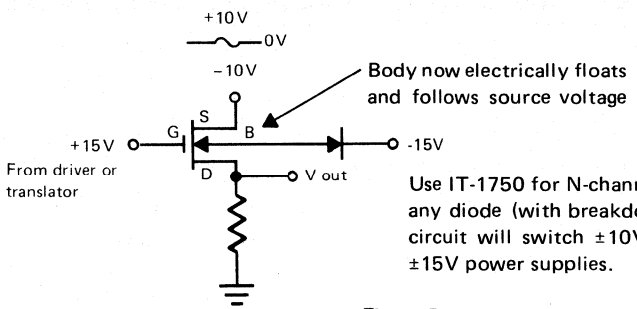
Figure C

To see the significance of this equation, look at Fig. A case. Here V_{bs} = -25V; the square root of 25V is 5. Then 2.5 X 5 = 12.5V.

Then with only 5V of gate to source enhancement, the channel is off when it is supposed to be on. Even if you got a low threshold device (i.e., a V_{th} of 1 to 2V measured with V_{bs} = 0) the circuit would not work properly. Actually the switch will not even begin to function until the signal voltage is about to 0V or below (Fig. B or C).

Another potential problem with this conventional circuit is that there is no overvoltage protection to prevent damaging the MOSFET during overvoltage spikes. For example, if the signal input should accidentally go below -15V you will forward bias the source to body junction. Since there is nothing to limit the forward biased current, severe MOSFET damage (probable failure) can result.

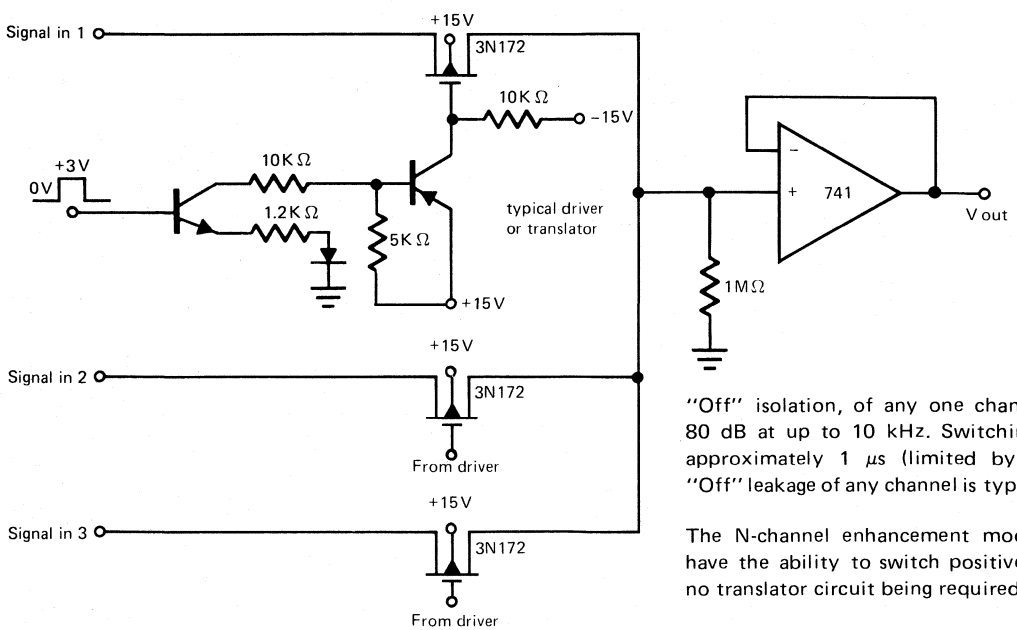
The solution to all these problems is to electrically float the body of the MOSFET. Fig. D shows the configuration. Now the V_{bs} = 0V because of the action of the back to back diodes. Also the configuration provides automatic overvoltage protection to + and -25V (if the diode breakdown is a minimum of 40V).



Use IT-1750 for N-channel MOSFET and any diode (with breakdown >40V). This circuit will switch ±10V ac signals with ±15V power supplies.

Figure D

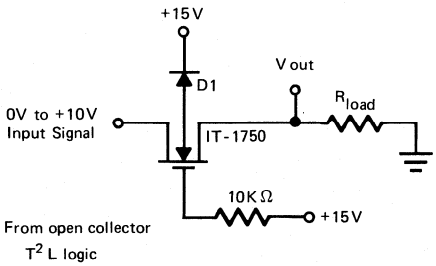
Multiplexing with the 3N172



"Off" isolation, of any one channel, is about 80 dB at up to 10 kHz. Switching speeds are approximately 1 μs (limited by the driver). "Off" leakage of any channel is typically 100 pa.

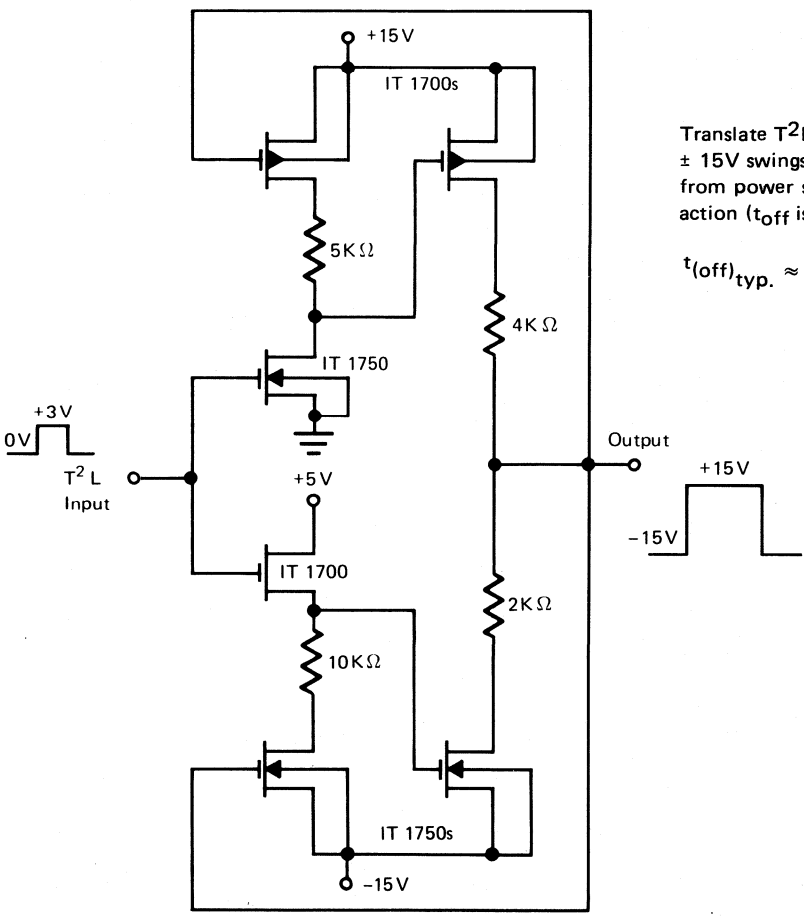
The N-channel enhancement mode MOSFETs have the ability to switch positive signals with no translator circuit being required.

Using the IT-1750 to switch 0V to +10V signals, without a driver.



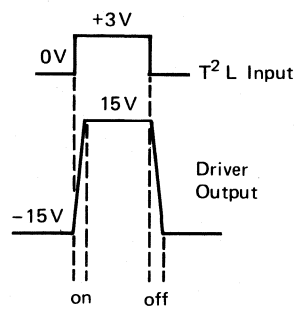
Note:
Addition of diode D1. This effectively floats body of MOSFET to provide overvoltage protection and keep "on" resistance constant.

High performance voltage translator circuit.



Translate T^2L levels (0V ⎍ +3V) into ± 15V swings. Draws no quiescent power from power supplies. Break before make action (t_{off} is much faster than t_{on}).

$t_{(off)_{typ.}} \approx 400$ ns, $t_{(on)_{typ.}} \approx 800$ ns



Actually circuit will take any input in -15V to +15V range and translate to fixed ± 15V output swings. Minimum turn-on voltage is 2.5V; maximum turn-off voltage is 0.4V.

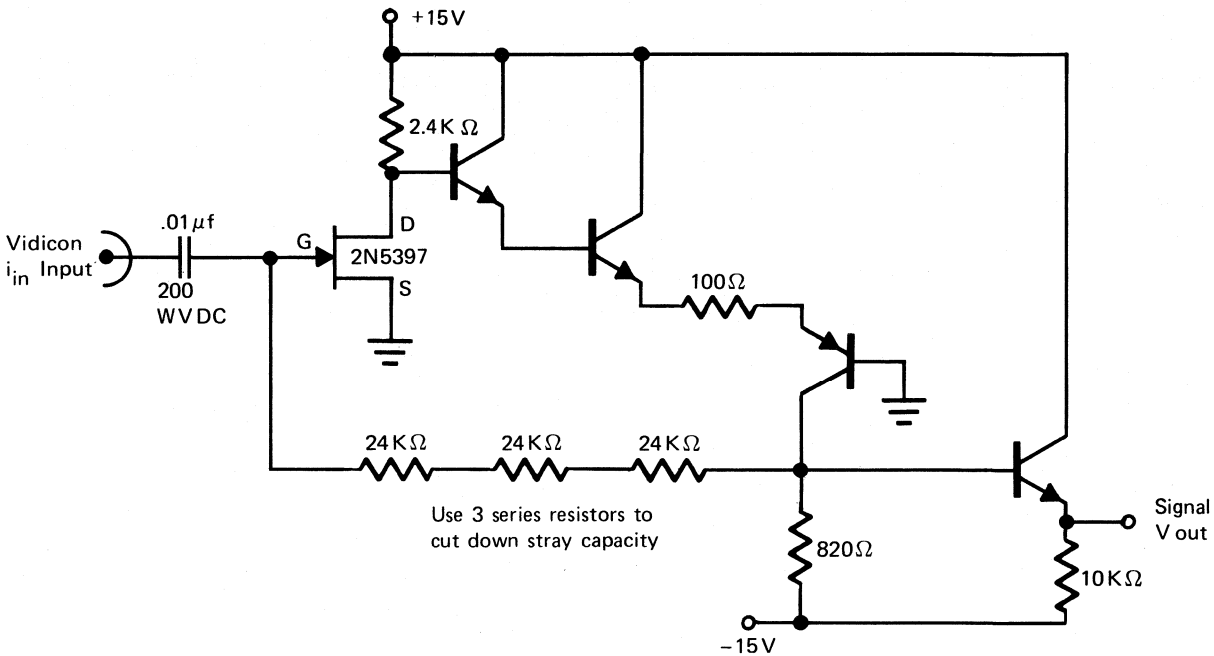
CATEGORY C: AMPLIFIERS—N-CHANNEL JUNCTION FET

N channel junction Field Effect Transistors designed for use in amplifier applications. Key parameters are g_{fs}, g_{iss}, g_{os}, I_g, I_{dss}, C_{iss}, C_{rss}, $V_{gs(off)}$, NF, $\bar{e}_n$ and i_n.

Ordering Information: Preferred Part Number	Package	G_{FS} min μmho	I_{DSS} min/max mA	V_p min/max V	I_{GSS} max pA	B_{VGSS} min V	C_{ISS} max pf	C_{RSS} max pf	$\bar{e}_n$ max nV/$\sqrt{Hz}$
2N3654	TO-72 TO-92	2000	2.5 7.5	-2.0 -5.0	-100	-50	4	1.2	140 @ 100 Hz
2N3655	TO-72 TO-92	1500	1.0 3.0	-1.0 -3.5	-100	-50	4	1.2	140 @ 100 Hz
2N3686	TO-72 TO-92	1000	0.4 1.2	-0.6 -2.0	-100	-50	4	1.2	140 @ 100 Hz
2N3687	TO-72 TO-92	500	0.1 0.5	-0.3 -1.2	-100	-50	4	1.2	140 @ 100 Hz
2N3822	TO-72 TO-92	3000	2.0 10.0	-6.0	-100	-50	6	3.0	200 @ 10 Hz
2N4117	TO-72 TO-92	70	0.03 0.09	-0.6 -1.8	-10	-40	3	1.5	
2N4117A	TO-72 TO-92	70	0.03 0.09	-0.6 -1.8	-1	-40		1.5	
2N4118	TO-72 TO-92	80	0.08 0.24	-1.0 -3.0	-10	-40	3	1.5	
2N4118A	TO-72 TO-92	80	0.08 0.24	-1.0 -3.0	-1	-40	3	1.5	
2N4119	TO-72 TO-92	100	0.2 0.6	-2.0 -6.0	-10	-40	3	1.5	
2N4119A	TO-72 TO-92	100	0.2 0.6	-2.0 -6.0	-1	-40	3	1.5	
2N4220	TO-72 TO-92	1000	0.5 3.0	-4.0	-100	-30	6	2.0	
2N4221	TO-72 TO-92	2000	2.0 6.0	-6.0	-100	-30	6	2.0	
2N4222	TO-72 TO-92	2500	5.0 15.0	-8.0	-100	-30	6	2.0	
2N4223	TO-72	3000	3.0 18.0	-0.1 -8.0	-250	-30	6	2.0	
2N4224	TO-72	2000	2.0 20.0	-0.1 -0.8	-150	-30	6	2.0	
2N4338	TO-18 TO-92	600	0.2 0.6	-0.3 -1.0	-100	-50	7	3.0	65 @ 1 kHz
2M4330	TO-18 TO-92	800	0.5 1.5	-0.6 -1.8	-100	-50	7	3.0	65 @ 1 kHz
2N4340	TO-18 TO-92	1300	1.2 3.6	-1.0 -3.0	-100	-50	7	3.0	65 @ 1 kHz
2N4341	TO-18 TO-92	2000	3.0 9.0	-2.0 -6.0	-100	-50	7	3.0	65 @ 1 kHz
2N4416	TO-72 TO-92	4500	5.0 15.0	-6.0	-100	-30	4	2.0	
2N4867	TO-72 TO-92	700	0.4 1.2	-0.7 -0.2	-250	-40	25	5.0	10 @ 1 kHz
2N4867A	TO-72 TO-92	700	0.4 1.2	-0.7 -2.0	-250	-40	25	5.0	5 @ 1 kHz
2N4868	TO-72 TO-92	1000	1.0 3.0	-1.0 -3.0	-250	-40	25	5.0	10 @ 1 kHz
2N4868A	TO-72 TO-92	1000	1.0 3.0	-1.0 -3.0	-250	-40	25	5.0	5 @ 1 kHz
2N4869	TO-72 TO-92	1300	2.5 7.5	-1.8 -5.0	-250	-40	25	5.0	10 @ 1 kHz
2N4869A	TO-72 TO-92	1300	2.5 7.5	-1.8 -5.0	-250	-40	25	5.0	5 @ 1 kHz
2N5397	TO-72 TO-92	600 @ 1 mA	10.0 30.0	-1.0 -6.0	-100	-25	5	1.2	3 dB @ 450 mHz
2N5457	TO-92	1000	1.0 5.0	-0.5 -6.0	1 nA	25	7	3.0	3 dB @ 450 mHz
2N5458	TO-92	1500	2.0 9.0	-1.0 -7.0	1 nA	25	7	3.0	3 dB @ 450 mHz
2N5459	TO-92	2000	4.0 16.0	-2.0 -8.0	-1 nA	-25	7	3.0	3 dB @ 450 mHz
2N5484	TO-92	3000	1.0 5.0	-0.3 -3.0	-1 nA	-25	5	1.0	120 @ 1 kHz
2N5485	TO-92	3500	4.0 10.0	-0.5 -4.0	-1 nA	-25	5	1.0	120 @ 1 kHz
2N5486	TO-92	4000	8.0 20.0	-2.0 -6.0	-1 nA	-25	5	1.0	120 @ 1 kHz
U308	TO-52 TO-92	10,000	12.0 60.0	-1.0 -6.0	-150	-25	7 typ.	4.0 typ.	10 @ 10 Hz typ.
U309	TO-52 TO-92	10,000	12.0 30.0	-1.0 -4.0	-150	-25	7 typ.	4.0 typ.	10 @ 10 Hz typ.
U310	TO-52 TO-92	10,000	24.0 60.0	-2.5 -6.0	-150	-25	7 typ.	4.0 typ.	10 @ 10 Hz typ.
UC200	TO-72 TO-92	6000	10.0 30.0	-6.0	-100	-50	7	3.0	70 @ 100 Hz

APPLICATION TIPS ON CATEGORY C

These N-channel J-FETs are usually used in amplifier applications. Key features are low noise with high source impedances and extremely high input impedance. Vidicon head preamplifiers for 10 mHz system.



Transresistance is ($V_{out} = i_{in} \times 72K$) giving a stage gain of 10 (voltage gain of 10) after the signal out point produces a transresistance of $V_{out} = i_{in} \times 720K\Omega$. Typical wide band noise (10 Hz to 10 mHz) is 6 mV RMS and 500 kHz to 10 mHz noise component is about 2.5 pA/mHz.

CATEGORY D: AMPLIFIERS—P-CHANNEL JUNCTION FET

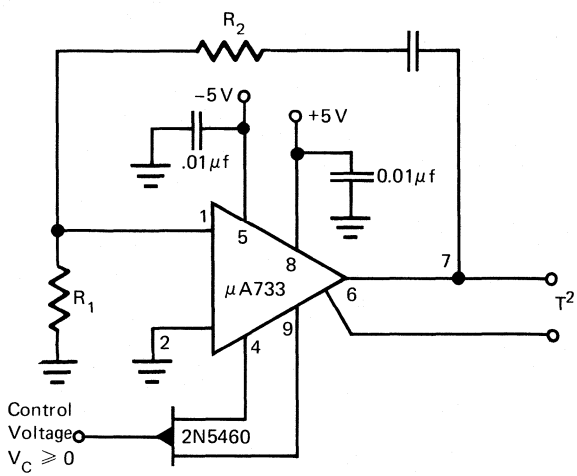
P channel junction Field Effect Transistors designed for use in amplifier applications. Key parameters are the same as those specified for N channel FETs.

Ordering Information: Preferred Part Number	Package	GFS min μmho	IDSS min/max mA	Vp min/max V	IGSS max nA	BVGSS min V	CISS max pf	CRSS max pf	$\bar{e}_n$ max nV/√Hz
2N2606	TO-18 TO-92	110	-0.1 -0.5	1.0 4.0	1	30	7	2	400 @ 1 kHz
2N2607	TO-18 TO-92	330	-0.3 -1.5	1.0 4.0	3	30	7	2	400 @ 1 kHz
2N2608	TO-18 TO-92	1000	-0.9 -4.5	1.0 4.0	10	30	7	2	180 @ 1 kHz
2N2609	TO-18 TO-92	2500	-2.0 -10.0	1.0 4.0	30	30	7	2	180 @ 1 kHz
2N3329	TO-72	1000 @ -1 mA	-1.0 -3.0	5.0	10	20	7	2	400 @ 1 kHz
2N3330	TO-72	1500 @ -2 mA	-2.0 -6.0	6.0	10	20	7	2	400 @ 1 kHz
2N3331	TO-72	2000 @ -5 mA	-5.0 -15.0	8.0	10	20	7	2	400 @ 1 kHz
2N5265	TO-72	900	-0.5 -1.0	3.0	2	60	7	2	115 @ 100 Hz
2N5266	TO-72	1000	-0.8 -1.6	3.0	2	60	7	2	115 @ 100 Hz
2N5267	TO-72	1500	-1.5 -3.0	6.0	2	60	7	2	115 @ 100 Hz
2N5268	TO-72	2000	-2.5 -5.0	6.0	2	60	7	2	115 @ 100 Hz
2N5269	TO-72	2200	-4.0 -8.0	8.0	2	60	7	2	115 @ 100 Hz
2N5270	TO-72	2500	-7.0 -14.0	8.0	2	60	7	2	115 @ 100 Hz
2N5460	TO-92	1000	-1.0 -5.0	0.75 6.0	5	40	7	2	115 @ 100 Hz
2N5461	TO-92	1500	-2.0 -9.0	1.0 7.5	5	40	7	2	115 @ 100 Hz
2N5462	TO-92	2500	-4.0 -16.0	1.5 9.0	5	40	7	2	115 @ 100 Hz
2N5463	TO-92	1000	-1.0 -5.0	0.75 6.0	5	60	7	2	115 @ 100 Hz
2N5464	TO-92	1500	-2.0 -9.0	1.0 7.5	5	60	7	2	115 @ 100 Hz
2N5465	TO-92	2500	-4.0 -16.0	1.8 9.0	5	60	7	2	115 @ 100 Hz

APPLICATION TIPS ON CATEGORY D

These P-channel Junction FETs are used in general purpose amplifier applications.

Voltage Controlled Oscillator



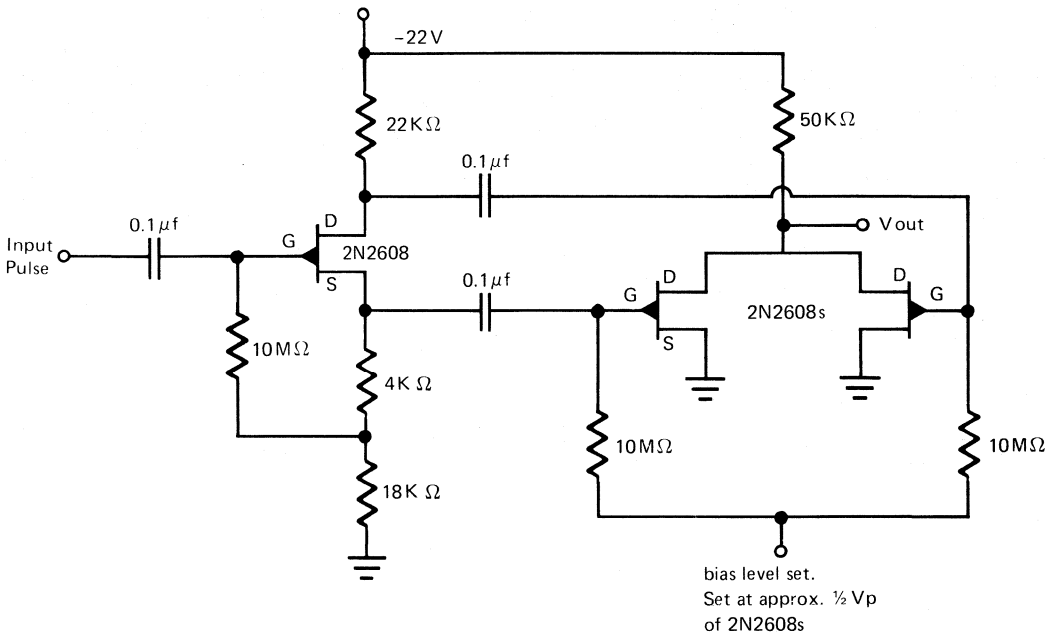
T = period of oscillation = $2C(R_1 + R_2)$

Set A_V = 10 on the μA733

Keep $\frac{R_1}{R_2}$ ration between 0.2 & 0.4

Set in $\left[A_V\ R_1/R_1 + R_2\right] \geq 2$

Simple voltage squaring circuit using the 2N2608s.



CATEGORY E: DIFFERENTIAL AMPLIFIERS—DUAL MONOLITHIC N-CHANNEL JUNCTION FETS

N channel dual monolithic Field Effect Transistors designed for use in high performance differential amplifier applications. Key parameters are (V_{gs1}-V_{gs2}), $\Delta(V_{gs1}-V_{gs2})/\Delta T$, I_{g1}-I_{g2}, g_{fs}, g_{fs1}/g_{fs2}, I_g, CMRR and $V_{gs(off)}$MAX.

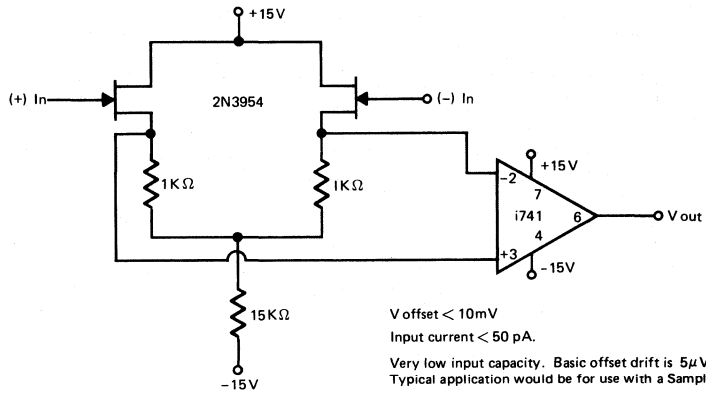
Ordering Information: Preferred Part Number	Package	VGS1-2 max mV	ΔVGS max μV/°C	I_G max pA	BVGSS min V	Vp min/max V	g_{fs} min/max μmho	IDSS min/max mA	$\bar{e}_n$ max nV/√Hz
2N3954	TO-71	5	10	-50	-50	-1.0 -4.5	1 4	0.5 5.0	160 @ 100 Hz
2N3954A	TO-71	5	5	-50	-50	-1.0 -4.5	1 4	0.5 5.0	160 @ 100 Hz
2N3955	TO-71	10	25	-50	-50	-1.0 -4.5	1 4	0.5 5.0	160 @ 100 Hz
2N3955A	TO-71	10	15	-50	-50	-1.0 -4.5	1 4	0.5 5.0	160 @ 100 Hz
2N3956	TO-71	15	50	-50	-50	-1.0 -4.5	1 4	0.5 5.0	160 @ 100 Hz
2N3957	TO-71	20	75	-50	-50	-1.0 -4.5	1 4	0.5 5.0	160 @ 100 Hz
2N3958	TO-71	25	100	-50	-50	-1.0 -4.5	1 4	0.7 7.0	160 @ 100 Hz
2N5196	TO-71	5	5	-15	-50	-0.7 -4.0	700 @ 200 μA	0.7 7.0	20 @ 1 kHz
2N5197	TO-71	5	10	-15	-50	-0.7 -4.0	700 @ 200 μA	0.7 7.0	20 @ 1 kHz
2N5198	TO-71	10	20	-15	-50	-0.7 -4.0	700 @ 200 μA	0.7 7.0	20 @ 1 kHz
2N5199	TO-71	15	40	-15	-50	-0.7 -4.0	700 @ 200 μA	0.7 7.0	20 @ 1 kHz
2N5452	TO-71	5	5	IGSS -100	-50	-1.0 -4.5	1 4	0.5 5.0	20 @ 1 kHz
2N5453	TO-71	10	10	IGSS -100	-50	-1.0 -4.5	1 4	0.5 5.0	20 @ 1 kHz
2N5454	TO-71	15	25	IGSS -100	-50	-1.0 -4.5	1 4	0.5 5.0	20 @ 1 kHz
2N5515	TO-71	5	5	-100	-40	-0.7 -4.0	1 4	0.5 7.5	30 @ 10 Hz
2N5516	TO-71	5	10	-100	-40	-0.7 -4.0	1 4	0.5 7.5	30 @ 10 Hz
2N5517	TO-71	10	20	-100	-40	-0.7 -4.0	1 4	0.5 7.5	30 @ 10 Hz
2N5518	TO-71	15	40	-100	-40	-0.7 -4.0	1 4	0.5 7.5	30 @ 10 Hz
2N5519	TO-71	15	80	-100	-40	-0.7 -4.0	1 4	0.5 7.5	30 @ 10 Hz
2N5520	TO-71	5	5	-100	-40	-0.7 -4.0	1 4	0.5 7.5	15 @ 10 Hz
2N5521	TO-71	5	10	-100	-40	-0.7 -4.0	1 4	0.5 7.5	15 @ 10 Hz
2N5522	TO-71	10	20	-100	-40	-0.7 -4.0	1 4	0.5 7.5	15 @ 10 Hz
2N5523	TO-71	15	40	-100	-40	-0.7 -4.0	1 4	0.5 7.5	15 @ 10 Hz
2N5524	TO-71	15	80	-100	-40	-0.7 -4.0	1 4	0.5 7.5	15 @ 10 Hz
2N5902	TO-99	5	5	-3	-40	-0.6 -4.5	70 250	0.3 0.5	100 @ 1 kHz
2N5903	TO-99	5	10	-3	-40	-0.6 -4.5	70 250	0.03 0.5	100 @ 1 kHz
2N5904	TO-99	10	20	-3	-40	-0.6 -4.5	70 250	0.03 0.5	100 @ 1 kHz
2N5905	TO-99	15	40	-3	-40	-0.6 -4.5	70 250	0.03 0.5	100 @ 1 kHz
2N5906	TO-99	5	5	-1	-40	-0.6 -4.5	70 250	0.03 0.5	100 @ 1 kHz
2N5907	TO-99	5	10	-1	-40	-0.6 -4.5	70 250	0.03 0.5	100 @ 1 kHz
2N5908	TO-99	10	20	-1	-40	-0.6 -4.5	70 250	0.03 0.5	100 @ 1 kHz
2N5909	TO-99	15	40	-1	-40	-0.6 -4.5	70 250	0.03 0.5	100 @ 1 kHz
2N5911	TO-99	10	20	-100	-25	-1.0 -5.0	5/10 @ 5 mA	7.0 40.0	20 @ 10 kHz
2N5912	TO-99	15	40	-100	-25	-1.0 -5.0	5/10 @ 5 mA	7.0 40.0	20 @ 10 kHz
SU2365	TO-71	5	10	-100	-30	-3.5	1/2 @ 200 μA	0.5 10.0	15 @ 1 kHz
SU2365A	TO-71	5	10	-20	-30	-3.5	1/2 @ 200 μA	0.5 10.0	50 @ 1 kHz
SU2366	TO-71	10	10	-100	-30	-3.5	1/2 @ 200 μA	0.5 10.0	15 @ 1 kHz
SU-2366A	TO-71	10	10	-20	-30	-3.5	1/2 @ 200 μA	0.5 10.0	50 @ 1 kHz
SU2367	TO-71	10	25	-100	-30	-3.5	1/2 @ 200 μA	0.5 10.0	15 @ 1 kHz
SU-2367A	TO-71	10	25	-20	-30	-3.5	1/2 @ 200 μA	0.5 10.0	50 @ 1 kHz
SU2368	TO-71	15	25	-100	-30	-3.5	1/2 @ 200 μA	0.5 10.0	15 @ 1 kHz
SU2368A	TO-71	15	25	-20	-30	-3.5	1/2 @ 200 μA	0.5 10.0	50 @ 1 kHz
U257	TO-99	100	–	-100	-25	-1.0 -5.0	5/10 @ 5 mA	5.0 40.0	30 @ 1 kHz

PRODUCT-BY-CATEGORY LISTING: CATEGORY E

APPLICATION TIPS ON CATEGORY E

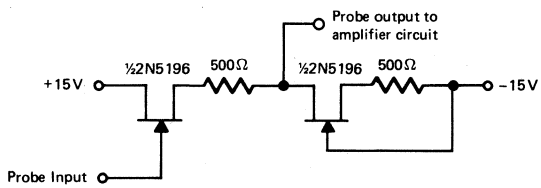
The monolithic, dual N-channel J-FETs are ideal for differential amplifier or input probe use.

Using the 2N3954 to make a FET front end operational amplifier.



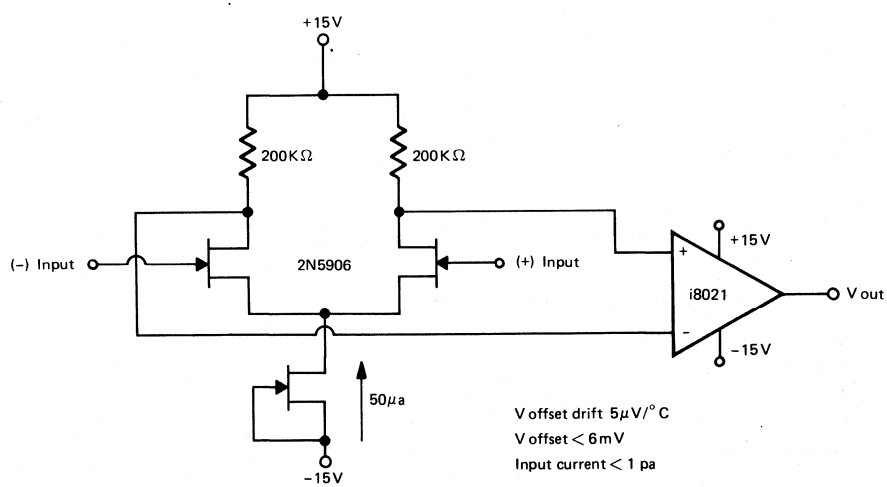
V offset < 10mV
Input current < 50 pA.
Very low input capacity. Basic offset drift is 5μV/°C + 741 offset drift.
Typical application would be for use with a Sample & Hold circuit.

Using the 2N5196 as a virtually no offset probe for voltmeter use (high impedance input probe and low capacity).



V offset < 5mV
V offset drift 5μV/°C
Input current < 15 pa

Using the 2N5906 to make a micropower amplifier. Key features are μa quiescent current and <1 pA input current.



V offset drift 5μV/°C
V offset < 6mV
Input current < 1 pa

CATEGORY F: DIFFERENTIAL AMPLIFIERS—DUAL MONOLITHIC P-CHANNEL MOSFETS (ENHANCEMENT)

P channel dual monolithic enhancement mode MOSFETs designed for ultra-low current amplifier applications.

Key parameters are I_g, $V_{gs(th)}$, C_{dg}.

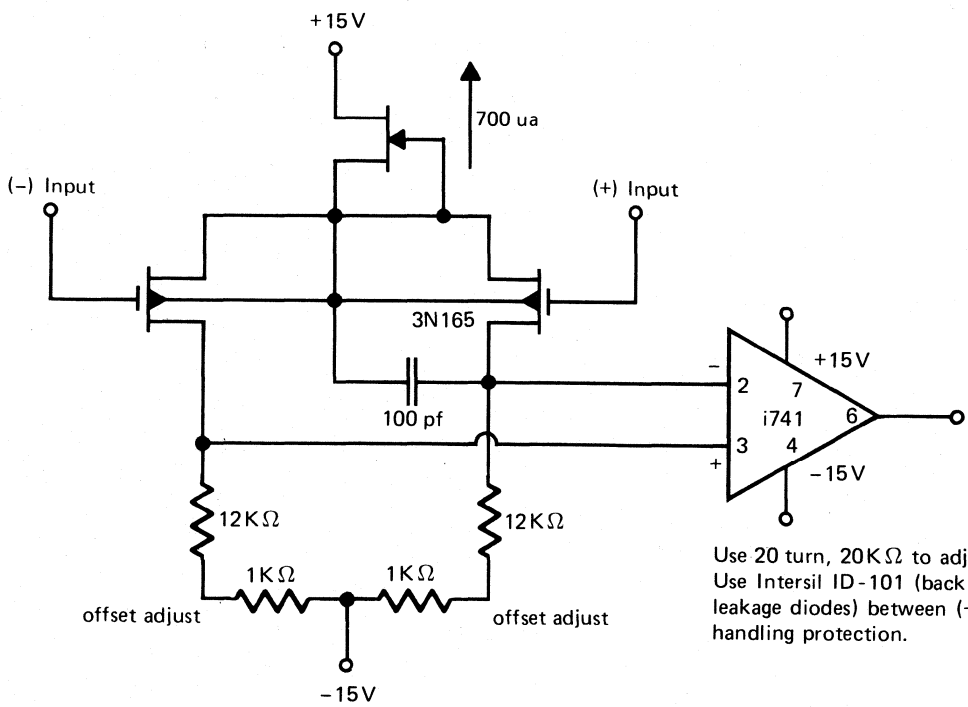
Ordering Information: Preferred Part Number	Package	$V_{GS\ (TH)}$ min/max V	B_{VDSS} min/max V	IDSS max pA	IGSS max pA	GFS min μ mho	ID (on) min/max mA	RDS (on) max ohm	VGS1-2 max mV
3N165	TO-99	-2 -5	-40	-200	-10	1500	-5.0 -30	300	100
3N166	TO-99	-2 -5	-40	-200	-10	1500	-5.0 -30	300	
3N188	TO-99	-2 -5	-40	-200	-200	1500	-5.0 -30	300	100 Zener Protected
3N189	TO-99	-2 -5	-40	-200	-200	1500	-5.0 -30	300	Zener Protected
3N190	TO-99	-2 -5	-40	-200	-200	1500	-5.0 -30	300	
3N191	TO-99	-2 -5	-40	-200	-200	1500	-5.0 -30	300	
MEM550	TO-99	-3 -6	-30	-10 nA	-10 nA	500	-1.5	250	Zener Protected

APPLICATION TIPS ON CATEGORY F

The monolithic, dual, P-channel, enhancement mode MOSFET pair is ideal for electrometer use. Proper handling and cleaning can result in consistently less than 0.01 pa input currents.

The part can also be utilized to make an intrusion detector which detects the charge given off as a result of friction of shoes with the floor.

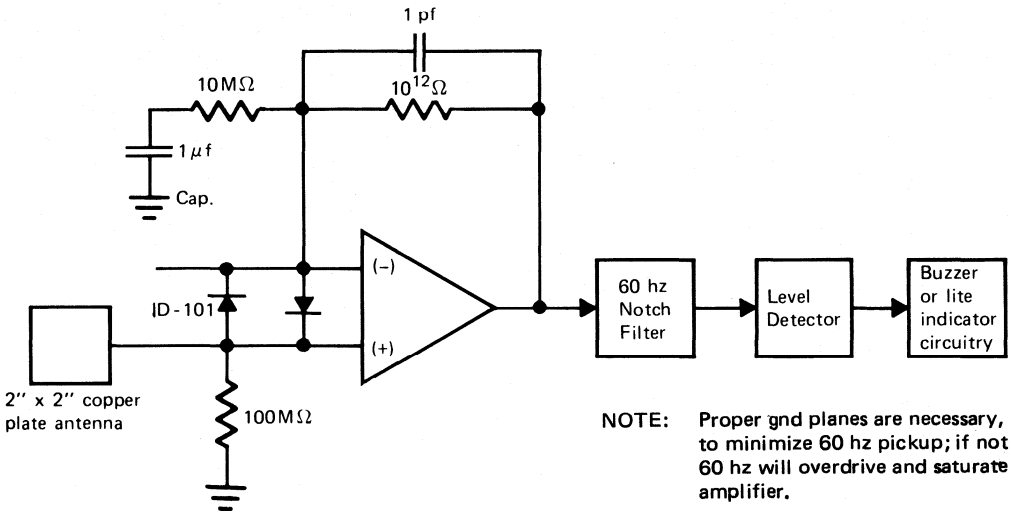
0.01 pa electrometer circuit input stage



Use 20 turn, 20KΩ to adjust offset to 0 mV. Use Intersil ID-101 (back to back super low leakage diodes) between (+) and (-) inputs for handling protection.

PRODUCT-BY-CATEGORY LISTING: CATEGORY F

Intrusion detection system utilizing the amplifier discussed in 0.01 pa electrometer circuit input stage. This describes how to construct an electrometer operational amplifier. Lets designate the system to be the usual operational amplifier block diagram and build up the intrusion system.



NOTE: Proper gnd planes are necessary, to minimize 60 hz pickup; if not 60 hz will overdrive and saturate amplifier.

CATEGORY G: DIFFERENTIAL AMPLIFIERS—DUAL MONOLITHIC BIPOLAR TRANSISTORS

Monolithic dual NPN and PNP Bipolar transistors designed for use in high performance differential amplifiers, operational amplifiers and transconductance multipliers. Key parameters are V_{be1}–V_{be2}, C_{ob}, NF, $\Delta(V_{be1}-V_{be2})/\Delta T$, and log conformance.

Ordering Information: Preferred Part Number	Package	V_{BE1-2} mV max	ΔV_{BE} $\mu V/^{\circ}C$ max	H_{FE} @ $I_C = 10\mu A$ $V_{CE} = 5V$ min	I_{B1-2} @ $I_C = 10\mu A$ $V_{CE} = 5V$ nA max	LV_{CEO} V min	I_{CBD} nA max	Noise dB max	f_t MHz @ I_C min	C_{obo} pf max	Structure	Type
2N2453	TO-78	3	10	80		30	5	7	150 @ 1 mA	8	Junc. Isol.	NPN
2N2453A	TO-78	3	5	80	.6 μA @ 100 μA	60	5	4	150 @ 1 mA	4	Junc. Isol.	NPN
2N4044	TO-78	3	3	200	5	60	.1	2	200 @ 1 mA	.8	Dielec. Isol.	NPN
2N4045	TO-78	5	10	80	25	45	.1	3	150 @ 1 mA	.8	Dielec. Isol.	NPN
2N4100	TO-78	5	5	150	10	55	.1	3	150 @ 1 mA	.8	Dielec. Isol.	NPN
2N4878	TO-71	3	3	200	5	60	.1	2	200 @ 1 mA	.8	Dielec. Isol.	NPN
2N4879	TO-71	5	5	150	10	55	.1	3	150 @ 1 mA	.8	Dielec. Isol.	NPN
2N4880	TO-71	5	10	80	25	45	.1	3	150 @ 1 mA	.8	Dielec. Isol.	NPN
2N5117	TO-78	.3	3	100	10	45	.1	4	100 @ .5 mA	.8	Dielec. Isol.	PNP
2N5118	TO-78	5	5	100	15	45	.1	4	100 @ .5 mA	.8	Dielec. Isol.	PNP
2N5119	TO-78	5	10	50	40	45	.1	4	100 @ .5 mA	.8	Dielec. Isol.	PNP
IT120	TO-78 TO-71	2	5	200	5	45	1	2 typ.	150 @ 1 mA	2	Junc. Isol.	NPN
IT120A	TO-78 TO-71	1	3	200	2.5	60	1	2 typ.	150 @ 1 mA	2	Junc. Isol.	NPN
IT121	TO-78 TO-71	5	10	80	10	45	1	2 typ.	150 @ 1 mA	2	Junc. Isol.	NPN
IT122	TO-78 TO-71	10	20	80	25	45	1	2 typ.	150 @ 1 mA	2	Junc. Isol.	NPN
IT124	TO-78	5	10	1500	.6 A V_{CE} = IV	2	.1	3	100 @ 200 μA	.8	Dielec. Isol.	NPN
IT126	TO-78 TO-71	1	3	200	2.5	60	.1	1 typ.	250 @ 10 mA	4	Dielec. Isol.	NPN
IT127	TO-78 TO-71	2	5	200	5	45	.1	1 typ.	250 @ 10 mA	4	Dielec. Isol.	NPN
IT128	TO-78 TO-71	5	10	100	10	45	.5	1 typ.	250 @ 10 mA	4	Dielec. Isol.	NPN
IT129	TO-78 TO-71	10	20	100	25	45	.5	1 typ	250 @ 10 mA	4	Dielec. Isol.	NPN
IT130	TO-78 TO-71	2	5	200	5	–45	1	2 typ	150 @ 1 mA	2	Junc. Isol.	PNP
IT130A	TO-78 TO-71	1	3	200	2.5	–60	1	2 typ.	150 @ 1 mA	2	Junc. Isol.	PNP
IT131	TO-78 TO-71	5	10	80	10	–45	1	2 typ.	150 @ 1 mA	2	Junc. Isol.	PNP
IT132	TO-78 TO-71	10	20	80	25	–45	1	2 typ.	150 @ 1 mA	2	Junc. Isol.	PNP
IT136	TO-78 TO-71	1	3	200	2.5	–60	.1	2 typ.	250 @ 10 mA	4	Dielec. Isol.	PNP
IT137	TO-78 TO-71	2	5	200	5	–45	.1	2 typ	250 @ 10 mA	4	Dielec. Isol.	PNP
IT138	TO-78 TO-71	5	10	100	10	–45	.5	2 typ.	250 @ 10 mA	4	Dielec. Isol.	PNP
IT139	TO-78 TO-71	10	20	100	25	–45	.5	2 typ.	250 @ 10 mA	4	Dielec. Isol.	PNP

Specialty Items

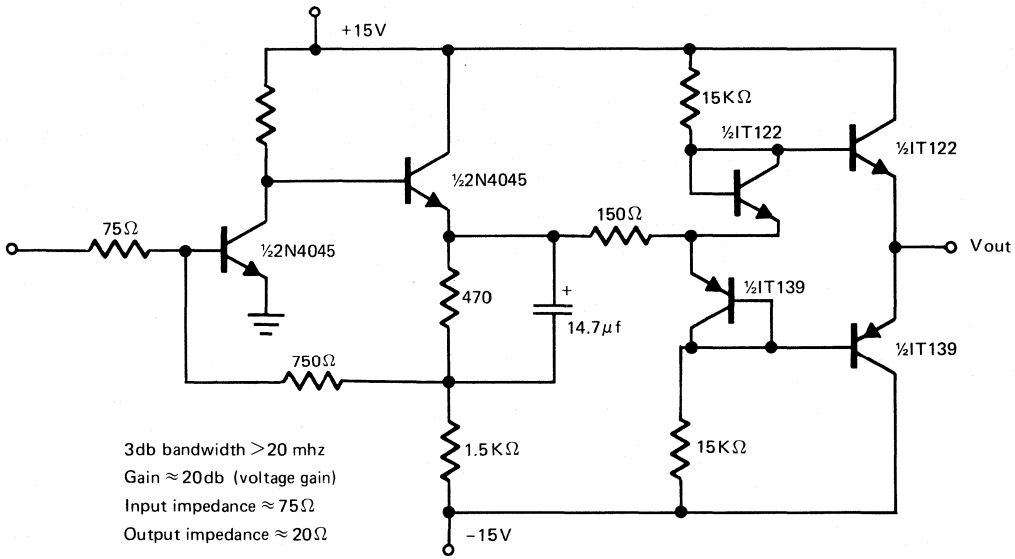
ID-100 ID-101	This product is a back to back diode combination used to protect P-channel MOSFET duals (non-diode protected). Their chief characteristic is $<$ 1 pa leakage when voltage across them is less than 5 mV. If voltage across diodes is adjusted to 0V $\pm$0.1 mV, leakage is less than 0.01 pa.

PRODUCT-BY-CATEGORY LISTING: CATEGORY G

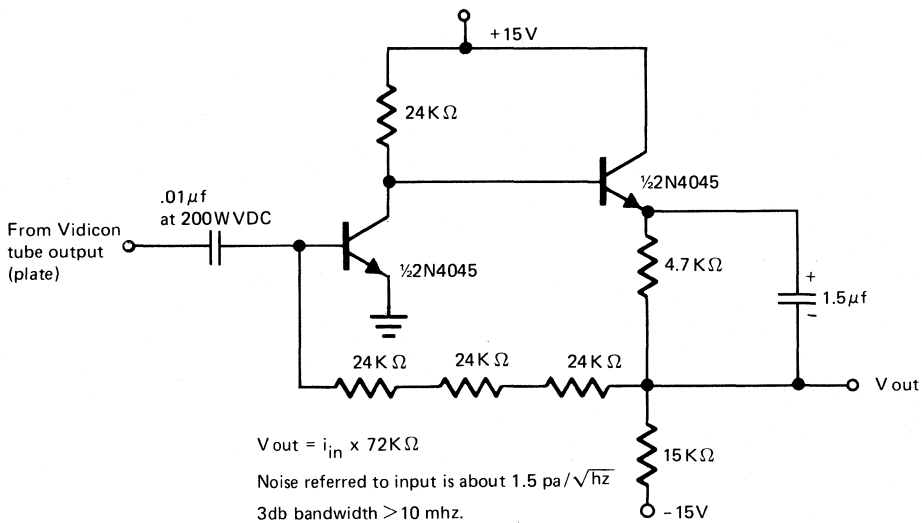
APPLICATION TIPS ON CATEGORY G

These dual monolithic, bipolar transistor pairs are excellent for high frequency amplifiers, vidicon head amplifiers, and high frequency buffer use.

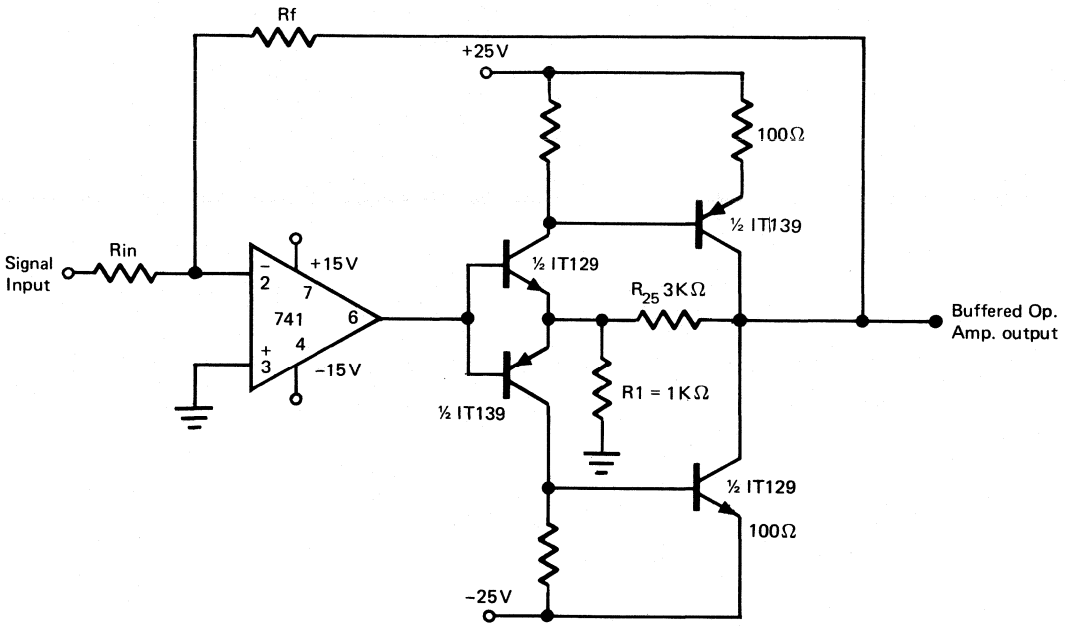
Using the monolithic bipolars to make a 20 mHz video amplifier which has 75Ω input impedance and drives 75Ω coax lines.



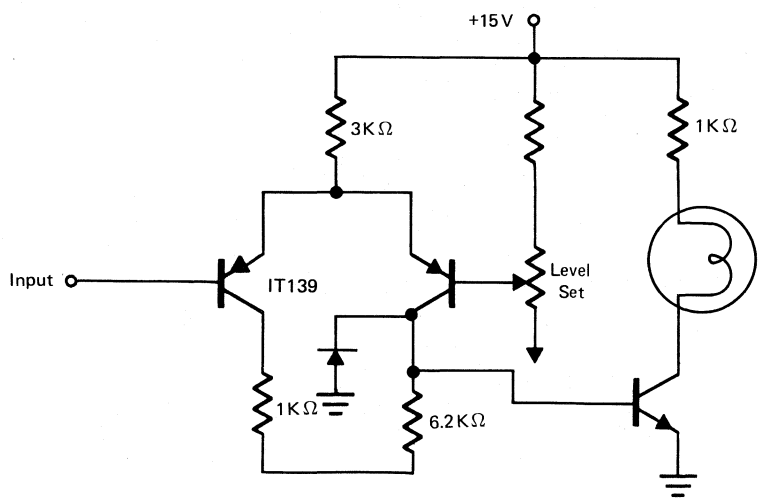
Using the 2N4045 to make a super low noise vidicon head preamplifier



Op Amp System using the IT129 and IT139.

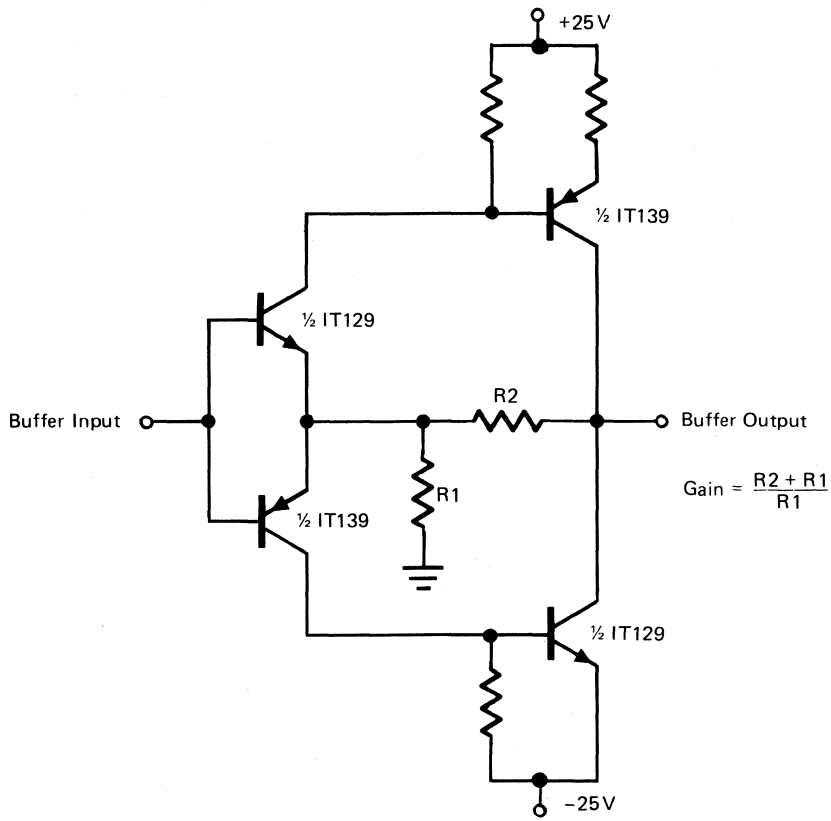


Level detector using the IT-139.



LED or other indicator to indicate when level has been detected. Light is off if Input level is below set level (±5 mV).

A power amplifier with gain; can be used to boost the signal handling capability of any operational amplifier, i.e., buffer output allows one to drive up to 50 mA output currents. The fact that the buffer has gain allows the designer to use a 741 with supply voltage of ± 15V and buffer with supply voltage of ± 25V and get ± 20V output swings.



FET, MOSFET AND DUAL TRANSISTOR CHIPS

INTRODUCTION

Intersil recognizes the increasing need for transistors and FETs in die form. To fulfill this need Intersil offers the entire line of JFETs, MOSFETs, and dual transistors in die form.

Die sales do, however, present some unique problems. In many cases the chips cannot be guaranteed to the same electrical specifications as the packaged part. This is caused by the fact that leakage, noise, AC parameters and temperature testing cannot be tested to the same degree of accuracy on dice as it can on packaged devices. This is due to equipment limitations and handling problems.

PURCHASE OPTIONS

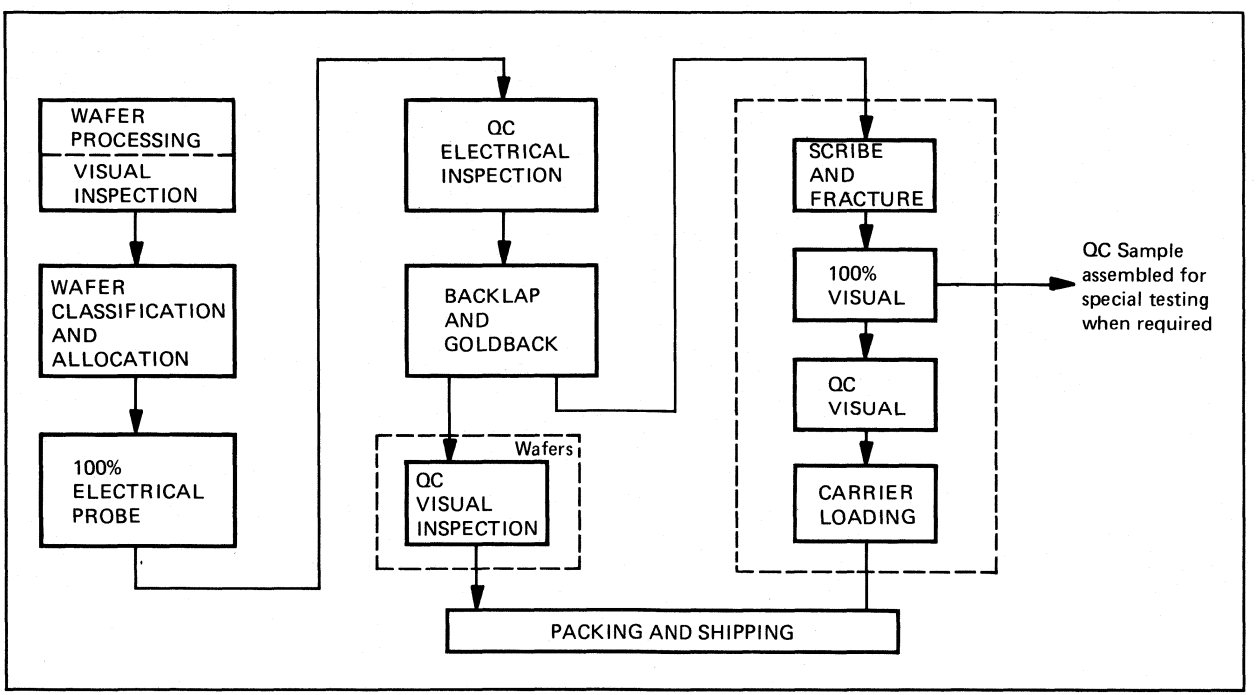
Intersil offers dice which are delivered in a number of forms:

- Chips which have been electrically probed, inked, visually inspected and diced.
- Wafers which have been electrically probed, inked, visually inspected and scribed only.
- Wafers which have been electrically probed, inked, and visually inspected only.

GENERAL PHYSICAL INFORMATION

- Chips are available with exact length X width dimensions plus tolerance (see individual data sheets). Chip height ranges from .003" to .006".
- To facilitate die attaching, chips are gold backed. Approximate thickness is 1000 angstroms. In general dice should be attached to gold, platinum, or palladium metallization. Thin-film gold, moly-gold and most of the thick-film metallization materials are compatible.
- Consult the individual data sheets for dimensions. Except for the aluminum bonding pads, the chips are completely covered with vapox (silicon dioxide). This minimizes damage to the chip caused by handling problems.
- All chips have aluminum metallization and aluminum bonding pads. Typical aluminum thickness is 12,000 angstroms.
- Die are 100% tested to electrical specifications, then visually inspected. When wafers are ordered, dice which fail the electrical test are inked out.
- Generally the minimum size of the die-attaching pad metallization should be at least 5 mils larger (on every edge) than the chip dimensions. For example, a 15 mil chip should be attached on at least a 25 mil pad.

CHIP AND WAFER PROCESSING FLOW CHART



FET, MOSFET AND DUAL TRANSISTOR CHIPS

RECOMMENDED DICE ASSEMBLY PROCEDURE

CLEANING:

Dice supplied in die form do not require cleaning prior to assembly. Dice supplied in wafer form should be cleaned after scribing and breaking. Freon TF in a vapor degreaser is the preferred cleaning method. However, an alternative is boiling the die in TCE for five minutes with a rinse in isopropyl alcohol for 1-2 minutes.

DIE ATTACH:

The die attach operation should be done under a gaseous nitrogen ambient to prevent oxidation. A preform should be used if the mounting surface has less than 50 microinches of gold and the die should be handled on the edges with tweezers. Die attach temperature should be between 385°C and 400°C with eutectic visible on three sides of the die after attach.

BONDING:

Thermocompression gold ball or aluminum ultrasonic bonding may be used. The gold ball should be about 3 times the diameter of the gold wire. The ball should cover the bonding pad, but not excessively or it may short out surrounding metallization. 1-mil aluminum wire may be used on most dice, but should not be used if the assembled unit will be plastic encapsulated.

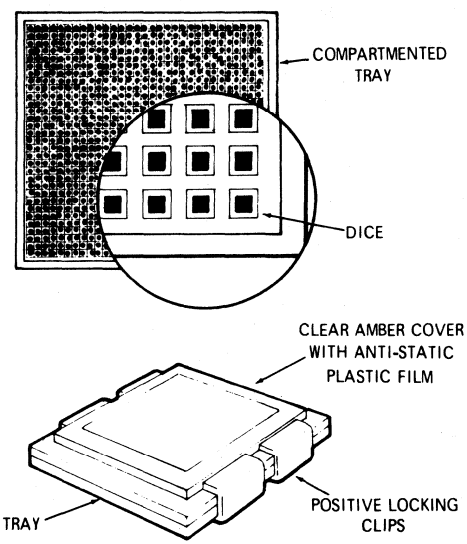
HANDLING OF DICE:

All dice shown in this catalog are passivated devices and Intersil warrants that they will meet or exceed published specifications when handled with the following precautions:

- Dice should be stored in a dry inert-gas atmosphere.
- Dice should be assembled using normal semiconductor techniques.
- Dice should be attached in a gaseous nitrogen spray at a temperature less than 430°C.

STANDARD DIE CARRIER PACKAGE

- Easy to handle, store and inventory.
- 100% electrically probed dice with electrical rejects removed.
- 100% visually sorted with mechanical and visual rejects removed.
- Easy visual inspection — dice in carriers, geometry side up.
- Individual compartment for each die.
- Carriers usuable in customer production area.
- Carrier may be storage container for unused dice.
- Carriers hold 25, 100, or 400 dice, depending on die size and quantity ordered.
- Part numbers shown in this catalog are for carrier packaging.



ELECTRICAL TEST LIMITATIONS – DUAL BIPOLAR TRANSISTORS

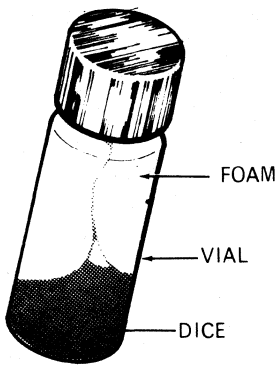
LV_{ceo}	100V max. @ ≤ 1 mA
BV_{cbo}	100V max. @ ≥ 1 μA
BV_{ebo}	100V max. @ ≤ 10 mA
H_{fe}	≤ 1000 @ ≥ 10 μA
$V_{ce(SAT)}$	≥ 10 mV @ ≤ 10 mA
I_{cbo}	≥ 100 pA @ ≤ 100V
$V_{be1} - V_{be2}$	≥ 1 mV @ ≥ 10 μA
$I_{b1} - I_{b2}$	≥ 2 nA

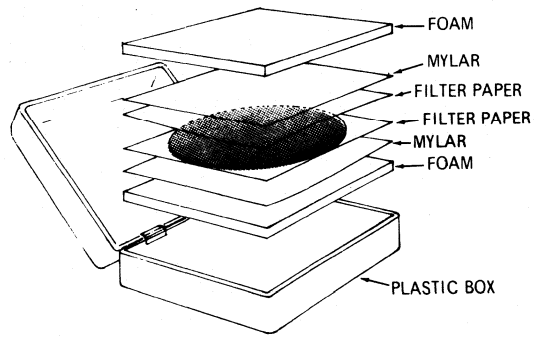
OPTIONAL VIAL PACKAGE

- 100% electrically probed dice with rejects inked but included in vial. Bulk shipment.
- 10% extra good dice included (no charge) to cover possible breakage and/or visual rejects.
- Preferred for production quantities.
- Lower cost.
- For vial package – replace "D" in catalog number with "V", e.g.: 2N4416/D (2N4416 dice in carrier) becomes 2N4416/V (2N4416 dice in vial).

OPTIONAL WAFER PACKAGE

- 100% electrically probed – rejects inked.
- 10% extra good dice included (no charge) to cover possible breakage and/or visual rejects.
- Preferred for production quantities.
- Lowest cost.
- Wafer is supplied unscribed.
- For wafer package – replace "D" in catalog type number with "W", e.g.: 2N4416/D (2N4416 dice in carrier) becomes 2N4416/W (2N4416 dice in wafer).





Note:
Intersil reserves the right to improve device geometries and manufacturing processes as required. These improvements may result in slight geometry changes. However, they will not affect the electrical limits, basic pad layouts or maximum die sizes in this catalog.

ELECTRICAL TEST LIMITATIONS – FETS

Breakdown voltage	100V max. @ 1 μA
Pinch-off voltage	0-20V @ $\geqslant$ 1 nA
$V_{GS(TH)}$	0-20V @ $\geqslant$ 10 μA
$R_{DS(on)}$	20Ω min. @ V_{GS} = 0 (V_{GS} = 30 MOSFETs)
I_{DSS} & $I_{D(on)}$	100 mA max.
gf_s	10,000 μMHOS max. @ $I_D \leqslant$ 10 mA
$I_{D(off)}$, $I_{S(off)}$, I_{GSS}	100 pA min.
$V_{GS1} - V_{GS2}$ (Duals)	10 mV min.

Electrical testing is guaranteed to a 10% LTPD. AC parameters such as capacitance and switching time cannot be tested in wafer or dice form.

FET, MOSFET AND DUAL TRANSISTOR CHIPS

ELECTRICAL TEST CAPABILITY

As an example of how to use the capability chart to see what Intersil actually guarantees and tests for, on a 100% basis, we compare the 2N4391 in a TO-18 package to the 2N4391 delivered as a chip.

Electrical Test Spec.	2N4391 in a TO-18	2N4391 Chip
I_{GSS} @ 25C	100 pA max.	100 pA max.
BV_{GSS}	40V min.	40V min.
$I_{D(off)}$ @ 25C	100 pA max.	100 pA max.
$V_{GS(forward)}$	1V max.	See note 1
$V_{GS(off)}$ or V_P	4V to 10V	4V to 10V
I_{DSS}	50 to 150 mA	50 to 100 mA
$V_{DS(on)}$	0.4V max.	0.4V max.
$r_{DS(on)}$	30Ω max.	30Ω max.
C_{iss}	14 pF max.	guaranteed by design
C_{rss}	3.5 pF max.	guaranteed by design
t_d	15 ns max.	guaranteed by design
t_r	5 ns max.	guaranteed by design
t_{off}	20 ns max.	guaranteed by design
t_f	15 ns max.	guaranteed by design

Note 1: This parameter is very dependent upon quality of metallization surface to which chip is attached.

SUMMARY

Of the 14 items specified for the package part, only 7 can be tested and guaranteed in die form. It is to be noted that those specifications which cannot be tested in die form can be sample tested in package form as an indicator of lot performance. Many of the tests, however, such as capacitance tests, are design parameters.

The above electrical testing is guaranteed to a 10% LTPD. However, there are occasions where customer requirements cannot be satisfied by wafer sort testing alone. While the previously described tests will be done on a 100% basis, Intersil recognizes the need for additional testing to obtain confidence that a particular customer's needs can be met with a reasonably high yield. Toward this end Intersil has instituted a dice sampling plan which is two-fold. First, random samples of the dice are packaged and tested to assure adherence to the electrical specification. When required, wafers are identified and wafer identity is tied to the samples. This tests both the electrical character of the die and its ability to perform electrically after going through the high temperature dice attachment stage. Second, more severe, testing can be performed on the packaged devices per individual customer needs. When testing other than that called out in the data sheet is required, Intersil issues an ITS number to describe the part. Examples of tighter testing which can be performed on packaged samples is shown below:

FET & Dual FET Pairs

1. Leakages to 1 pA (I_{gss})
2. $R_{DS(on)}$ to as low as 4 ohms
3. $I_{D(off)}$ to 10 pA
4. I_{DSS} to 1 amp (pulsed)
5. G_{FS} to 10,000 μmho
6. G_{os} to 1 μmho
7. $\bar{e}_n$ noise to 5 nV/$\sqrt{Hz}$ at frequencies of 10 Hz to 100 kHz
8. CMRR to 100 dB
9. $\Delta (V_{gs1}-V_{gs2})/\Delta T$ down to 10 μV/°C to an LTPD of 20%
10. g_m match to 5%
11. I_{DSS} match to 5%

Transistor Pairs

1. Leakages to as low as 1 pA
2. Beta with collector current up to 50 mA and as low as 100 nA
3. f_T up to 500 MHz with collector currents in the range of 10 μA to 10 mA
4. Noise measurements as low as 5 nV/$\sqrt{Hz}$ from 10 Hz to 100 kc
5. $\Delta (V_{be1}-V_{be2})/\Delta T$ to 10 μV/°C to an LTPD of 20%

Visual Inspection

Individual chips are 100% inspected to MIL-STD-750, Method 2072 or, as an option, MIL-STD-883, Level B. Inspection is done to an LTPD of 20%. As an option, Intersil offers S.E.M. capability on all wafers.

Discrete Semiconductor Data Sheets

FEATURES

- Closely Matched Current Gain
- Very Closely Matched, V_{BE}
- Low Differential Drift

Intersil

MONOLITHIC DUAL MATCHED NPN TRANSISTOR

2N2453 2N2453A

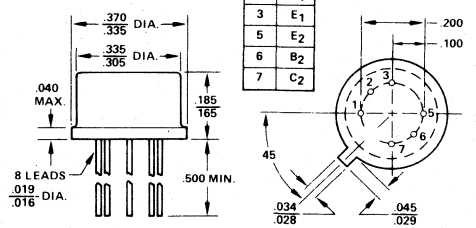
MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Collector-Base Voltage 2N2453 2N2453A	V_{CBO}	 60 80	Volts
Collector-Emitter Voltage 2N2453 2N2453A	V_{CEO}	 30 50	Volts
Emitter-Base Voltage	V_{EBO}	7.0	Volts
Total Device Dissipation @ T_A = 25°C @ T_C = 100°C @ T_C = 25°C	P_D	Each Side Both Sides 0.2 0.3 0.35 0.7 0.6 1.2	Watts
Storage Temperature	T_{stg}	−65 to +200	°C
Junction Temperature	T_J	+200	°C
Derating Factor above 25°C 2N2453 2N2453A		 1.14 1.71	mW/°C

PACKAGE DIMENSIONS

TO-78

PIN	OUT
1	C_1
2	B_1
3	E_1
5	E_2
6	B_2
7	C_2



4003

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER			MIN	MAX	UNIT	TEST CONDITIONS	
BV_{CBO}	Collector-Base Breakdown Voltage	2N2453 2N2453A	60 80		V	I_C = 10 μA, I_E = 0	
BV_{EBO}	Emitter-Base Breakdown Voltage		7.0		V	I_C = 0, I_E = 0.1 μA	
$V_{CEO(sus)}$**	Collector-Emitter Sustaining Voltage	2N2453 2N2453A	30 60		V	I_C = 10 mA, I_B = 0	
$V_{CE(sat)}$	Collector Saturation Voltage			1.0	V	I_C = 5.0 mA, I_B = 0.5 mA	
$V_{BE(sat)}$	Base Saturation Voltage			0.9	V	I_C = 5.0 mA, I_B = 0.5 mA	
I_{CBO}	Collector-Base Cutoff Current	2N2453 2N2453A 2N2453 2N2453A		5.0 5.0 10 10	nA μA 	I_E = 0, V_{CB} = 50 V I_E = 0, V_{CB} = 60 V I_E = 0, V_{CB} = 50 V I_E = 0, V_{CB} = 60 V	 T_A = 150°C T_A = 150°C
I_{EBO}	Emitter-Base Cutoff Current			2.0	nA	I_C = 0, V_{EB} = 5.0 V	
h_{FE}	DC Current Gain		80 40 150 75	600		I_C = 10 μA, V_{CE} = 5.0 V I_C = 10 μA, V_{CE} = 5.0 V I_C = 1.0 mA, V_{CE} = 5.0 V I_C = 1.0 mA, V_{CE} = 5.0 V	 T_A = −55°C T_A = −55°C
h_{FE1}/h_{FE2}*	DC Current Gain Ratio	2N2453A only Both Types Both Types	0.9 0.9 0.85	1.0 1.0 1.0		I_C = 100 μA, V_{CE} = 5.0 V I_C = 1.0 mA, V_{CE} = 5.0 V I_C = 1.0 mA, V_{CE} = 5.0 V	 T_A = −55°C to +125°C
$V_{BE1}-V_{BE2}$	Base Voltage Differential			5.0 3.0	mV	I_C = 1.0 mA, V_{CE} = 5.0 V I_C = 10 μA, V_{CE} = 5.0 V	
$\Delta(V_{BE1}-V_{BE2})/\Delta T$	Base Voltage Differential Drift	2N2453 2N2453A		10 5.0	μV/°C	I_C = 10 μA, V_{CE} = 5.0 V	T_A = −55°C to +125°C
h_{fe}	Small Signal Current Gain		150	600		I_C = 1.0 mA, V_{CE} = 5.0 V	f = 1 kHz
$\|h_{fe}\|$	High Frequency Current Gain		2.0			I_C = 5.0 mA, V_{CE} = 10 V	f = 30 MHz
C_{ob}	Output Capacitance	2N2453 2N2453A		8.0 4.0	pF	I_E = 0, V_{CB} = 10 V	f = 140 kHz
C_{ib}	Input Capacitance			10	pF	I_C = 0, V_{BE} = 0.5 V	f = 140 kHz
h_{rb}	Voltage Feedback Ratio			5.0	x10^{-4}	I_C = 1.0 mA, V_{CE} = 5.0 V	f = 1 kHz
h_{re}	Reverse Voltage Feedback Ratio			6.0	x10^{-4}	I_C = 1.0 mA, V_{CE} = 5.0 V	f = 1 kHz
h_{ib}	Input Resistance		20	30	ohms	I_C = 1.0 mA, V_{CB} = 5.0 V	f = 1 kHz
h_{ie}	Input Resistance			5.0	kΩ	I_C = 1.0 mA, V_{CE} = 5.0 V	f = 1 kHz
h_{ob}	Output Conductance			0.2	μmhos	I_C = 1.0 mA, V_{CB} = 5.0 V	f = 1 kHz
h_{oe}	Output Conductance		5.0	30	μmhos	I_C = 1.0 mA, V_{CB} = 5.0 V	f = 1 kHz
NF	Low Frequency Noise Figure	2N2453 2N2453A		7.0 4.0	dB	f = 1 kHz Source resistance = 10 kΩ Equivalent noise power bandwidth = 200 Hz I_C = 10 μA, V_{CE} = 5.0 V	

*The lower of the h_{FE} readings is taken as h_{FE1}.
**Pulse Test: Pulse Width = 300 μsec; Duty Cycle = 1%.

Intersil

P-CHANNEL
SILICON PLANAR
EPITAXIAL J-FET

2N2606 2N2607 2N2608 2N2609

GENERAL DESCRIPTION

- Low-level Choppers
- Data Switches
- Commutators

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	-65°C to +200°C
Operating Junction Temperature	+175°C
Lead Temperature (Soldering, 10 sec. time limit)	+260°C

Maximum Power Dissipation

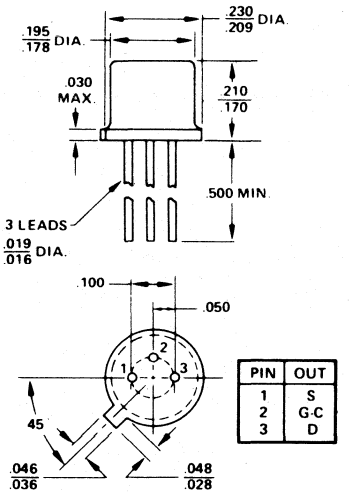
Device Dissipation @ Free Air Temperature	300 mW
Linear Derating	2.0 mW/°C

Maximum Voltages & Current

V_{DG}	Drain to Gate Voltage	30 V
V_{SG}	Source to Gate Voltage	30 V
I_G	Gate Current	50 mA

PACKAGE DIMENSIONS

TO-18



ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

Characteristic		Test Conditions		2N2606		2N2607		2N2608		2N2609		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
I_{GSS}	Gate-Source Cutoff Current †	V_{GS} = 30 V, V_{DS} = 0			1		3		10		30	nA
		V_{GS} = 5 V, V_{DS} = 0, T_A = 150° C			1		3		10		30	μA
BV_{GDS}	Gate-Drain Breakdown Voltage	I_G = 1 μA, V_{DS} = 0		30		30		30		30		V
V_P	Gate-Source Pinch-Off Voltage	V_{DS} = -5 V, I_D = -1 μA		1	4	1	4	1	4	1	4	V
I_{DSS}	Drain Current at Zero Gate Voltage	V_{DS} = -5 V, V_{GS} = 0		-0.10	-0.50	-0.30	-1.50	-0.90	-4.50	-2	-10	mA
g_{fs}	Small-Signal Common-Source Forward Transconductance	V_{DS} = -5 V, V_{GS} = 0, f = 1 kHz		110		330		1000		2500		μmho
C_{iss}	Gate-Source Input Capacitance	V_{DS} = -5 V, V_{GS} = 1 V, f = 140 kHz			6		10		17		30	pF
NF	Noise Figure	V_{DS} = -5 V, V_{GS} = 0, f = 1 kHz	R_G = 10 MΩ		3		3					dB
			R_G = 1 MΩ						3		3	

Intersil

P-CHANNEL
SILICON PLANAR
EPITAXIAL J-FET

2N3329 2N3330 2N3331

GENERAL DESCRIPTION

For
- Multi-Purpose Amplifiers
- Analog Multipliers
- Modulators

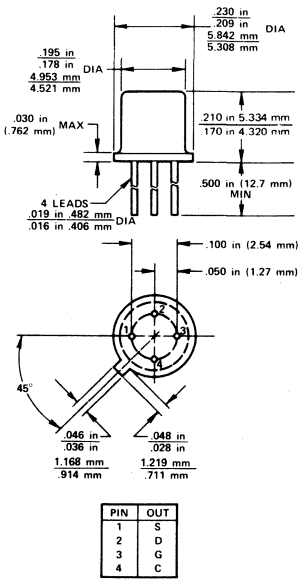
ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Gate-Drain and Gate-Source Voltage	20 V
Gate Current	10 mA
Total Device Dissipation at (or below) 25°C Free-Air Temperature	0.3 W
Storage Temperature Range	-65°C to +200°C
Lead Temperature (1/16" from case for 10 seconds)	230°C

PACKAGE DIMENSIONS

TO-72



PIN	OUT
1	S
2	D
3	G
4	C

5503B

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N3329 MIN	2N3329 MAX	2N3330 MIN	2N3330 MAX	2N3331 MIN	2N3331 MAX	UNITS	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		0.01		0.01		0.01	μA	V_{GS} = 10 V, V_{DS} = 0	
			10		10		10		V_{GS} = 10 V, V_{DS} = 0, T_A = 150°C	
BV_{GSS}	Gate-Source Breakdown Voltage	20		20		20		V	I_G = 10 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage		5		6		8		V_{DS} = -5 V, I_D = -10 μA	
I_{DSS}	Saturation Drain Current	-1	-3	-2	-6	-5	-15	mA	V_{DS} = -10 V, V_{GS} = 0	
$r_{DS(on)}$	Drain-Source ON Resistance		1000		800		600	Ω	I_D = -100 μA, V_{GS} = 0	
g_{is}	Common-Source Input Conductance		0.2		0.2		0.2	μmho	V_{DS} = -10 V, 2N3329: I_D = -1 mA, 2N3330: I_D = -2 mA, 2N3331: I_D = -5 mA	f = 1 kHz
g_{rs}	Common-Source Reverse Transfer Conductance		0.1		0.1		0.1			
g_{os}	Common-Source Output Conductance		20		40		100			
g_{fs}	Common-Source Forward Transconductance	1000	2000	1500	3000	2000	4000			
		900		1350		1800				f = 10 MHz
C_{iss}	Common-Source Input Capacitance		20		20		20	pF	V_{DS} = -10 V, V_{GS} = 1 V	f = 1 MHz
NF	Noise Figure		3		3		4	dB	V_{DS} = -5 V, I_D = -1 mA, R_{gen} = 1 MΩ	f = 1 kHz
NF	Noise Figure								V_{DS} = -5 V, I_D = -1 mA, R_{gen} = 10 MΩ	f = 10 Hz

Intersil

N-CHANNEL
SILICON PLANAR
EPITAXIAL J-FET

2N3684 2N3685
2N3686 2N3687

FEATURES

- $C_{GSS} < 1.2$ pF

GENERAL DESCRIPTION

- Exceptionally high figure of merit
- Radiation Immunity
- Symmetrical devices for low-level choppers, data switches, multiplexers and low noise amplifiers
- Extremely low noise and capacitance
- High input impedance
- Zero offset
- High reliability silicon epitaxial planar construction

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	TO-72	−65°C to +200°C
Storage Temperature	TO-92	−55°C to +125°C
Operating Junction Temperature	TO-72	+200°C
Operating Junction Temperature	TO-92	+125°C
Lead Temperature (Soldering, 10 sec time limit)		+260°C

Maximum Power Dissipation

Device Dissipation @ Free Air Temperature	300 mW
Linear Derating TO-72	1.7 mW/°C
TO-92	3.0 mW/°C

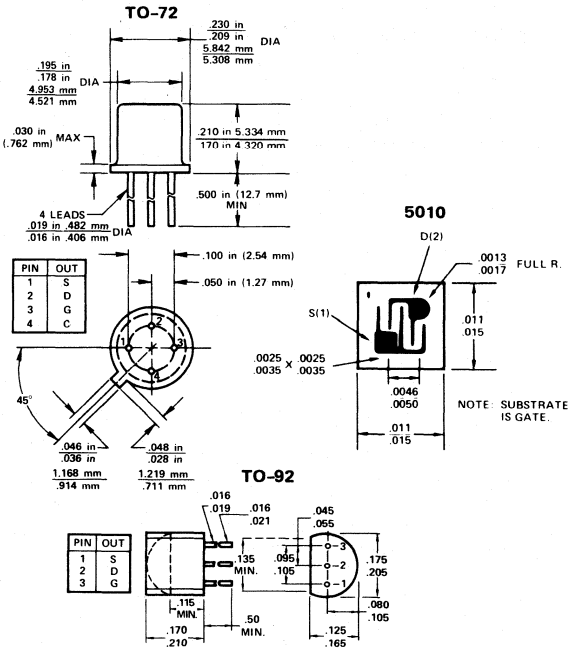
Maximum Voltages & Current

V_{GS}	Gate to Source Voltage	−50 V
V_{GD}	Gate to Drain Voltage	−50 V
I_G	Gate Current	50 mA

ORDERING INFORMATION

TO72	TO92	WAFER	CHIP
2N3684	2N3684-TO92	2N3684/W	2N3684/D
2N3685	2N3685-TO92	2N3685/W	2N3685/D
2N3686	2N3686-TO92	2N3686/W	2N3686/D
2N3687	2N3687-TO92	2N3687/W	2N3687/D

PACKAGE DIMENSIONS



ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

PARAMETER		2N3684		2N3685		2N3686		2N3687		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
BV_{GSS}	Gate to Source Breakdown Voltage	−50		−50		−50		−50		V	V_{DS} = 0 V, I_G = 1.0 μA
V_P	Pinch-Off Voltage	2.0	5.0	1.0	3.5	0.6	2.0	0.3	1.2	V	V_{DS} = 20 V, I_D = 0.001 μA
I_{GSS}	Total Gate Leakage Current		−0.1		−0.1		−0.1		−0.1	nA	V_{GS} = −30 V, V_{DS} = 0
I_{GSS}	Total Gate Leakage Current (150°C)		−0.5		−0.5		−0.5		−0.5	μA	V_{GS} = −30 V, V_{DS} = 0 @150°C
I_{DSS}	Saturation Current, Drain-to-Source	2.5	7.5	1.0	3.0	0.4	1.2	0.1	0.5	mA	V_{GS} = 0 V, V_{DS} = 20 V
$\|Y_{fs}\|$	Forward Transadmittance	2000	3000	1500	2500	1000	2000	500	1500	μmhos	V_{DS} = 20 V, V_{GS} = 0 V f = 1 kHz
C_{iss}	Common Source Input Capacitance (Output Shorted)		4.0		4.0		4.0		4.0	pF	V_{DS} = 20 V, V_{GS} = 0, f = 1 kHz
G_{os}	Small Signal, Common Source Output Conductance (input shorted)		50		25		10		5	μmhos	V_{DS} = 20 V, V_{GS} = 0, f = 1 kHz
C_{rss}	Small Signal, Common Source Short Circuit Reverse Transfer Capacitance		1.2		1.2		1.2		1.2	pF	V_{DS} = 20 V, V_{GS} = 0, f = 1 kHz
R_{on}	On Resistance		600		800		1200		2400	Ohms	V_{DS} = 0, V_{GS} = 0
NF	Noise Figure (Spot)		0.5		0.5		0.5		0.5	dB	f = 100 Hz, R_G = 10 MΩ NBW = 6 Hz, V_{DS} = 10 V

FEATURES

- Low Capacity
- Up to 6500 μmho Transconductance

Intersil

N-CHANNEL SILICON PLANAR EPITAXIAL J FET

2N3821
2N3822

GENERAL DESCRIPTION

For small signal amplifier and oscillator applications.

ORDERING INFORMATION

TO72	TO92	WAFER	CHIP
2N3821	2N3821-TO92	2N3821/W	2N3821/D
2N3822	2N3822-TO92	2N3822/W	2N3822/D

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	TO72	-65°C to +200°C
Storage Temperature	TO92	-55°C to +125°C
Operating Junction Temperature	TO72	+200°C
Operating Junction Temperature	TO92	+125°C
Lead Temperature (Soldering, 10 sec time limit)		+260°C

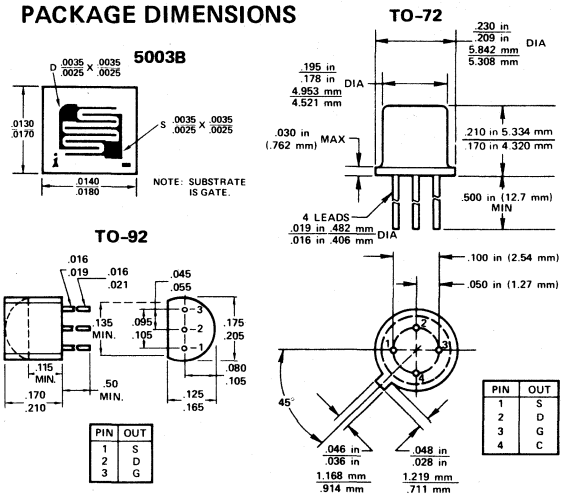
Maximum Power Dissipation

Device Dissipation @ Free Air Temperature	300 mW
Linear Derating TO72	1.7 mW/°C
TO92	3.0 mW/°C

Maximum Voltages & Current

V_{GS} Gate to Source Voltage	-50 V
V_{GD} Gate to Drain Voltage	-50 V
I_G Gate Current	10 mA

PACKAGE DIMENSIONS



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N3821 MIN	2N3821 MAX	2N3822 MIN	2N3822 MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		-0.1		-0.1	nA	V_{GS} = -30 V, V_{DS} = 0	
			-0.1		-0.1	μA		150°C
BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		V	I_G = -1 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage		-4		-6		V_{DS} = 15 V, I_D = 0.5 nA	
V_{GS}	Gate-Source Voltage	-0.5	-2				V_{DS} = 15 V, I_D = 50 μA	
				-1	-4		V_{DS} = 15 V, I_D = 200 μA	
I_{DSS}	Saturation Drain Current	0.5	2.5	2	10	mA	V_{DS} = 15 V, V_{GS} = 0 (Note 3)	
g_{fs}	Common-Source Forward Transconductance (Note 1)	1500	4500	3000	6500	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
$\|y_{fs}\|$	Common-Source Forward Transadmittance	1500		3000				f = 100 MHz
g_{os}	Common-Source Output Conductance (Note 1)		10		20			f = 1 kHz
C_{iss}	Common-Source Input Capacitance		6		6	pF		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		3		3			
NF	Noise Figure		5		5	dB	V_{DS} = 15 V, V_{GS} = 0, R_{gen} = 1 meg, BW = 5 Hz	f = 10 Hz
$\overline{e_n}$	Equivalent Input Noise Voltage		200		200	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 15 V, V_{GS} = 0, BW = 5 Hz	

NOTE:

1. These parameters are measured during a 2 msec interval 100 msec after d-c power is applied.

GENERAL DESCRIPTION

Matched FET pairs for differential amplifiers. This family of general purpose FETs is characterized for low and medium frequency differential amplifiers requiring low offset voltage, drift, noise, and capacitance.

MONOLITHIC DUAL, MATCHED N-CHANNEL J-FETS (PAIR)

2N3954 2N3954A 2N3955 2N3955A 2N3956 2N3957 2N3958

FEATURES

- Offset Voltage < 5 mV — 2N3954A
- Drift < 5 μV/°C
- Low Capacitance — C_{iss} = 4 pF Max
- Spot Noise Figure = 0.5 dB Max
- Superior Tracking Ability
- Low Output Conductance — g_{os} = 35 μmho Max

ABSOLUTE MAXIMUM RATINGS

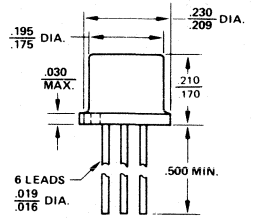
@ 25°C (unless otherwise noted)

Any Case-To-Lead Voltage	±100 V
Gate-Drain or Gate-Source Voltage	-50 V
Gate-To-Gate Voltage	±100 V
Gate Current	50 mA
Total Device Dissipation 85°C (Each Side)	250 mW
Case Temperature (Both Sides)	500 mW
Power Derating (Each Side)	2.86 mW/°C
(Both Sides)	4.3 mW/°C
Storage Temperature Range	−65°C to +125°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

ORDERING INFORMATION

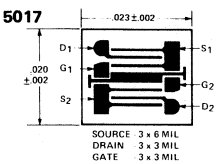
TO71	WAFER	CHIP
2N3954	2N3954/W	2N3954/D
2N2954A	2N3954A/W	2N3954A/D
2N3955	2N3955/W	2N3955/D
2N3955A	2N3955A/W	2N3955A/D
2N3956	2N3956/W	2N3956/D
2N3957	2N3957/W	2N3957/D
2N3958	2N3958/W	2N3958/D

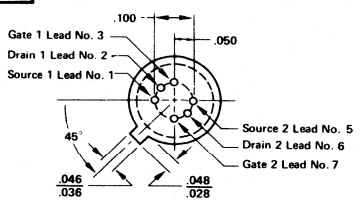
TO-71



PACKAGE DIMENSIONS

5017





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N3954		2N3954A		2N3955		2N3955A		2N3956		2N3957		2N3958		UNIT	TEST CONDITIONS	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
I_{GSS}	Gate Reverse Current		-100		-100		-100		-100		-100		-100		-100	pA	V_{GS} = -30 V,	
			-500		-500		-500		-500		-500		-500		-500	nA	V_{DS} = 0	T_A = 125°C
BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		-50		-50		-50		-50		-50		V	V_{DS} = 0 I_G = 1 μA	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1.0	-4.5	-1.0	-4.5	-1.0	-4.5	-1.0	-4.5	-1.0	-4.5	-1.0	-4.5	-1.0	-4.5	V	V_{DS} = 20 V, I_D = 1 nA	
$V_{GS(f)}$	Gate-Source Forward Voltage		2.0		2.0		2.0		2.0		2.0		2.0		2.0	V	V_{DS} = 0 I_G = 1 mA	
V_{GS}	Gate-Source Voltage		-4.2		-4.2		-4.2		-4.2		-4.2		-4.2		-4.2	V	V_{DS} = 20 V	I_D = 50 μA
		-0.5	-4.0	-0.5	-4.0	-0.5	-4.0	-0.4	-4.0	-0.5	-4.0	-0.5	-4.0	-0.5	-4.0	V		I_D = 200 μA
I_G	Gate Operating Current		-50		-50		-50		-50		-50		-50		-50	pA	V_{DS} = 20 V,	
			-250		-250		-250		-250		-250		-250		-250	nA	I_D = 200 μA	T_A = 125°C
I_{DSS}	Saturation Drain Current	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	mA	V_{DS} = 20 V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance	1000	3000	1000	3000	1000	3000	1000	3000	1000	3000	1000	3000	1000	3000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
		1000		1000		1000		1000		1000		1000		1000		μmho		f = 200 MHz
g_{os}	Common-Source Output Conductance		35		35		35		35		35		35		35	μmho		f = 1 kHz
C_{iss}	Common-Source Input Capacitance		4.0		4.0		4.0		4.0		4.0		4.0		4.0	pF		
C_{rss}	Common Source Reverse Transfer Capacitance		1.2		1.2		1.2		1.2		1.2		1.2		1.2	pF		f = 1 MHz
C_{dgo}	Drain-Gate Capacitance		1.5		1.5		1.5		1.5		1.5		1.5		1.5	pF	V_{DG} = 10 V, I_S = 0	
NF	Common-Source Spot Noise Figure		0.5		0.5		0.5		0.5		0.5		0.5		0.5	dB	V_{DS} = 20 V V_{GS} = 0 R_G = 10 MΩ	f = 100 Hz
$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		10		10		10		10		10		10		10	nA	V_{DS} = 20 V, I_D = 200 μA	T = 125°C
I_{DSS1}/I_{DSS2}	Drain Saturation Current Ratio	0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	0.90	1.0	0.85	1.0		V_{DS} = 20 V V_{GS} = 0	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5.0		5.0		10.0		5.0		15		20		25	mV	V_{DS} = 20 V, I_D = 200 μA	
$\Delta\lvert V_{GS1}-V_{GS2}\rvert$	Gate-Source Differential Voltage Change with Temperature		0.8		0.4		2.0		1.2		4.0		6.0		8.0	mV		T = 25°C to -55°C
			1.0		0.5		2.5		1.5		5.0		7.5		10.0	mV		T = 25°C to 125°C
g_{fs1}/g_{fs2}	Transconductance Ratio	0.97	1.0	0.97	1.0	0.97	1.0	0.95	1.0	0.95	1.0	0.90	1.0	0.85	1.0			f = 1 kHz

FEATURES

- Low $r_{DS(on)}$ – 150Ω Max (2N3993)
- High $|Y_{fs}|/C_{iss}$ Ratio (High-Frequency Figure-of-Merit)

Intersil

P–CHANNEL SILICON PLANAR EPITAXIAL J FET

2N3993
2N3994

GENERAL DESCRIPTION

Used in high-speed commutator and chopper applications. Also ideal for "Virtual Gnd" switching; needs no ext. translator circuit to switch ±10 VAC. Can be driven direct from T^2L or CMOS logic.

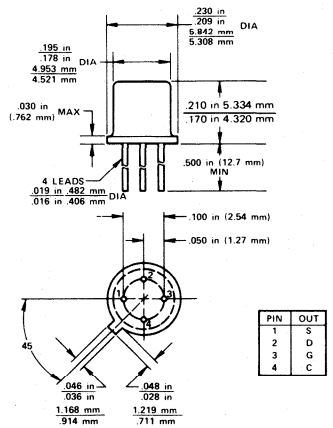
MAXIMUM RATINGS

@25°C free-air temperature (unless otherwise noted)

Drain-Gate Voltage	-25 V
Drain-Source Voltage	-25 V
Reverse Gate-Source Voltage	+25 V
Continuous Forward Gate Current	-10 mA
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 1)	300 mW
Storage Temperature Range	-65°C to 200°C
Lead Temperature 1/16 Inch from Case for 10 Seconds	300°C

PACKAGE DIMENSIONS

TO-72



5508B

*ELECTRICAL CHARACTERISTICS @ 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		2N3993 MIN	2N3993 MAX	2N3994 MIN	2N3994 MAX	UNIT
^{BV}GSS	Gate-Source Breakdown Voltage	I_G = 1 μA,	V_{DS} = 0	25		25		V
I_{DGO}	Drain Reverse Current	V_{DG} = -15 V,	I_S = 0		-1.2		-1.2	nA
		V_{DG} = -15 V,	I_S = 0, T_A = 150°C		-1.2		-1.2	μA
I_{DSS}	Zero-Gate-Voltage Drain Current	V_{DS} = -10 V,	V_{GS} = 0, See Note 2	-10		-2		mA
$I_{D(off)}$	Drain Cutoff Current	V_{DS} = -10 V,	V_{GS} = 6 V				-1.2	nA
		V_{DS} = -10 V,	V_{GS} = 6 V, T_A = 150°C				-1	μA
		V_{DS} = -10 V,	V_{GS} = 10 V		-1.2			nA
		V_{DS} = -10 V,	V_{GS} = 10 V, T_A = 150°C		-1			μA
$V_{GS(off)}$	Gate-Source Voltage	V_{DS} = -10 V,	I_D = -1 μA	4	9.5	1	5.5	V
$r_{ds(on)}$	Small-Signal Drain-Source On-State Resistance	V_{GS} = 0, f = 1 kHz	I_D = 0,		150		300	Ω
$\|y_{fs}\|$	Small-Signal Common-Source Forward Transfer Admittance	V_{DS} = -10 V, f = 1 kHz,	V_{GS} = 0, See Note 2	6	12	4	10	mmho
C_{iss}	Common-Source Short-Circuit Input Capacitance	V_{DS} = -10 V, f = 1 MHz,	V_{GS} = 0, See Note 3		16		16	pF
C_{rss}	Common-Source Short-Circuit Reverse Transfer Capacitance	V_{DS} = 0, f = 1 MHz	V_{GS} = 6 V,				5	pF
		V_{DS} = 0, f = 1 MHz	V_{GS} = 10 V,		4.5		4.5	pF

NOTES:

2. These parameters must be measured using pulse techniques. t_p = 100 ms, duty cycle ⩽ 10%.
3. This parameter must be measured with bias voltages applied for less than 5 seconds to avoid overheating.

*Indicates JEDEC registered data.

†The fourth lead (case) is connected to the source for all measurements.

FEATURES

- High Gain At Low Current $h_{FE} \geq 200$ @ 10 μA
- Low Output Capacitance $C_{obo} \leq 0.8$ pF
- h_{FE} Match $h_{FE_1} / h_{FE_2} \leq 10\%$
- Tight V_{BE} Tracking
  $\Delta (V_{BE_1} - V_{BE_2}) \leq 3\ \mu V/°C$ -55°C to +125°C
- Dielectrically isolated matched pairs for differential amplifiers.

Intersil

DUAL MONOLITHIC MATCHED NPN SILICON PLANAR TRANSISTORS

2N4044 2N4045 2N4100
2N4878 2N4879 2N4880

GENERAL DESCRIPTION

Dual monolithic matched NPN silicon planar transistors used for differential amplifier applications.

ORDERING INFORMATION

TO78	TO71	WAFER	CHIP
2N4044		2N4044/W	2N4044/D
2N4045		2N4045/W	2N4045/D
2N4100		2N4100/W	2N4100/D
	2N4878		
	2N4879		
	2N4880		

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	-65°C to +200°C
Operating Junction Temperature	+200°C

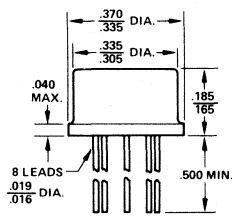
Maximum Power Dissipation

	TO-71		TO-78	
	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Total Dissipation at 25°C Case Temperature	0.3 Watt	0.5 Watt	0.4 Watt	0.75 Watt
Derating Factor	1.7mW/°	2.9mW/°C	2.3mW/°C	4.3mW/°C

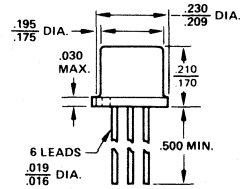
		2N4044 2N4878	2N4100 2N4879	2N4045 2N4880
V_{CBO}	Collector to Base Voltage	60 V	55 V	45 V
V_{CEO}	Collector to Emitter Voltage	60 V	55 V	45 V
V_{EBO}	Emitter to Base Voltage (Note 2)	7 V	7 V	7 V
V_{CCO}	Collector to Collector Voltage	100 V	100 V	100 V
I_C	Collector Current	10mA	10mA	10mA

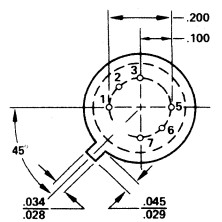
PACKAGE DIMENSIONS

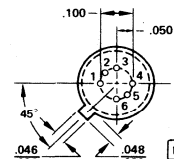
TO-78



TO-71

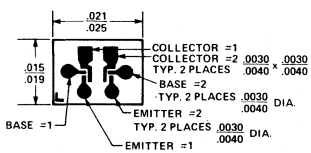






PIN	OUT
1	C_1
2	B_1
3	E_1
5	E_2
6	B_2
7	C_2

4000



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N4044 2N4878 MIN	2N4044 2N4878 MAX	2N4100 2N4879 MIN	2N4100 2N4879 MAX	2N4045 2N4880 MIN	2N4045 2N4880 MAX	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	200	600	150	600	80	800		I_C = 10 μA, V_{CE} = 5V
h_{FE}	DC Current Gain	225		175		100			I_C = 1.0 mA, V_{CE} = 5 V
h_{FE}(-55°C)	DC Current Gain	75		50		30			I_C = 10 μA, V_{CE} = 5 V
$V_{BE(on)}$	Emitter-Base On Voltage		0.7		0.7		0.7	V	I_C = 10 μA, V_{CE} = 5 V
$V_{CE(sat)}$	Collector Saturation Voltage		0.35		0.35		0.35	V	I_C = 1.0 mA, I_B = 0.1 mA
I_{CBO}	Collector Cutoff Current		0.1		0.1		0.1*	nA	I_E = 0, V_{CB} = 45 V, 30 V*
I_{CBO}(+150°C)	Collector Cutoff Current		0.1		0.1		0.1*	μA	I_E = 0, V_{CB} = 45 V, 30 V*
I_{EBO}	Emitter Cutoff Current		0.1		0.1		0.1	nA	I_C = 0, V_{EB} = 5 V
C_{obo}	Output Capacitance		0.8		0.8		0.8	pF	I_E = 0, V_{CB} = 5 V

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N4044 2N4878		2N4100 2N4879		2N4045 2N4880		UNIT	TEST CONDITIONS	
		MIN	MAX	MIN	MAX	MIN	MAX			
C_{TE}	Emitter Transition Capacitance		1		1		1	pF	$I_C = 0$, $V_{EB} = 0.5$ V	
C_{C_1, C_2}	Collector to Collector Capacitance		0.8		0.8		0.8	pF	$V_{CC} = 0$	
I_{C_1, C_2}	Collector to Collector Leakage Current		5		5		5	pA	$V_{CC} = \pm 100$ V	
$V_{CEO(sust)}$	Collector to Emitter Sustaining Voltage	60		55		45		V	$I_C = 1$ mA, $I_B = 0$	
f_T	Current Gain Bandwidth Product	200		150		150		MHz	$I_C = 1$ mA, $V_{CE} = 10$ V	
f_T	Current Gain Bandwidth Product	20		15		15		MHz	$I_C = 10\ \mu$A, $V_{CE} = 10$ V	
NF	Narrow Band Noise Figure		2		3		3	dB	$I_C = 10\ \mu$A, $V_{CE} = 5$ V $R_G = 10$ ohms	f = 1 kHz BW = 200 Hz
BV_{CBO}	Collector Base Breakdown Voltage	60		55		45		V	$I_C = 10\ \mu$A, $I_E = 0$	
BV_{EBO}	Emitter Base Breakdown Voltage	7		7		7		V	$I_E = 10\ \mu$A, $I_C = 0$	

MATCHING CHARACTERISTICS (25°C unless otherwise noted)

h_{FE_1}/h_{FE_2}	DC Current Gain Ratio (Note 3)	0.9	1	0.85		0.8	1		$I_C = 10\ \mu$A to 1 mA, $V_{CE} = 5$ V	
$\lvert V_{BE_1} - V_{BE_2} \rvert$	Base Emitter Voltage Differential		3		5		5	mV	$I_C = 10\ \mu$A, $V_{CE} = 5$ V	
$\lvert I_{B_1} - I_{B_2} \rvert$	Base Current Differential		5		10		25	nA	$I_C = 10\ \mu$A, $V_{CE} = 5$ V	
$\lvert \Delta(V_{BE_1} - V_{BE_2}) \rvert / °C$	Base-Emitter Voltage Differential Change with Temperature		3		5		10	μV/°C	$I_C = 10\ \mu$A, $V_{CE} = 5$ V	$T_A = -55°C$ to $+125°C$
$\lvert \Delta(I_{B_1} - I_{B_2}) \rvert / °C$	Base Current Differential Change with Temperature		0.3		0.5		1	nA/°C	$I_C = 10\ \mu$A, $V_{CE} = 5$ V	$T_A = -55°C$ to $+125°C$

SMALL SIGNAL CHARACTERISTICS

PARAMETER		TYPICAL VALUE	UNIT	TEST CONDITIONS
h_{ib}	Input Resistance	28	ohms	$I_C = 1$ mA, $V_{CB} = 5$ V
h_{rb}	Voltage Feedback Ratio	4.3	x 10^{-4}	$I_C = 1$ mA, $V_{CB} = 5$ V
h_{fe}	Small Signal Current Gain	250		$I_C = 1$ mA, $V_{CE} = 5$ V
h_{ob}	Output Conductance	0.6	x 10^{-7} mhos	$I_C = 1$ mA, $V_{CB} = 5$ V
h_{ie}	Input Resistance	9.6	k ohms	$I_C = 1$ mA, $V_{CE} = 5$ V
h_{re}	Voltage Feedback Ratio	4.2	x 10^{-4}	$I_C = 1$ mA, $V_{CE} = 5$ V
h_{oe}	Output Conductance	12	μmhos	$I_C = 1$ mA, $V_{CE} = 5$ V

NOTES:
1. These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.
2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed 10 μamps.
3. The lowest of two h_{FE} readings is taken as h_{FE_1} for purposes of this ratio.

FEATURES

- $r_{DS(ON)} < 30$ ohms (2N4091)
- $I_{D(OFF)} < 100$ pA (JAN TX Types)
- Fast Switching

Intersil

N–CHANNEL SILICON J FET

2N4091 JAN TX 2N4091
2N4092 JAN TX 2N4092
2N4093 JAN TX 2N4093

DESCRIPTION:

This family of junction FETs are characterized for analog switching applications requiring zero dc offset voltage, low ON resistance and fast switching speeds. The JAN TX versions are fully tested to meet the specifications of Mil-S-19500.

ORDERING INFORMATION

TO18	TO92	WAFER	CHIP
2N4091	2N4091-TO92	2N4091/W	2N4091/D
2N4092	2N4092-TO92	2N4092/W	2N4092/D
2N4093	2N4093-TO92	2N4093/W	2N4093/D
JAN TX 2N4091			
JAN TX 2N4092			
JAN TX 2N4093			

ABSOLUTE MAXIMUM RATINGS

(@25°C unless otherwise noted)

Maximum Temperatures

Storage Temperature	−55 to +200°C
Operating Junction Temperature	−55 to +175°C
Lead Temperature (soldering, 10 sec. limit)	300°C

Maximum Power Dissipation

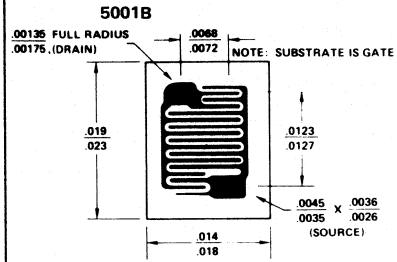
Device Dissipation @ Free Air Temperature	360 mW
Linear Derating (TO18)	10 mW/°C
(TO92)	16 mW/°C

Maximum Voltages & Currents

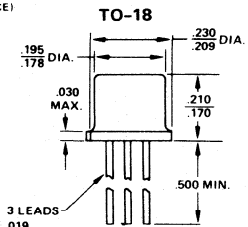
V_{GS} Gate to Source Voltage	−40 V
V_{DS} Drain to Source Voltage	−40 V
V_{DG} Drain to Gate Voltage	40 V
I_G Gate Current	10 mA

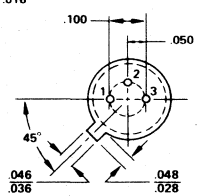
PACKAGE DIMENSIONS:

5001B



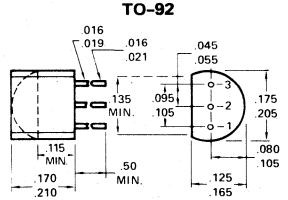
TO-18





PIN	OUT
1	S
2	D
3	G, C

TO-92



PIN	OUT
1	S
2	D
3	G

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

Characteristic			2N4091 Min.	2N4091 Max.	2N4092 Min.	2N4092 Max.	2N4093 Min.	2N4093 Max.	Unit	Test Conditions	
BV_{GSS}	Gate-Source Breakdown Voltage		−40		−40		−40		V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
I_{DGO}	Drain Reverse Current (Not JAN TX Specified)			200		200		200	pA	$V_{GS} = -20$ V, $I_S = 0$	25 C
				400		400		400	nA		150 C
I_{GSS}	Gate Reverse Current (JAN TX Only)			-100		-100		-100	pA	$V_{GS} = -20$ V, $V_{DS} = 0$	25 C
				-200		-200		-200	nA		150 C
$I_{D(OFF)}$	Drain Cutoff Current							100	pA	$V_{DS} = 20$ V	$V_{GS} = -6$ V, 25 C
								200	nA		150 C
		JAN TX Only				100			pA		$V_{GS} = -8$ V, 25 C
						200			nA		150 C
				100					pA		$V_{GS} = -12$ V, 25 C
				200					nA		150 C
								200	pA		$V_{GS} = -6$ V, 25 C
								400	nA		150 C
						200			pA		$V_{GS} = -8$ V, 25 C
						400			nA		150 C
				200					pA		$V_{GS} = -12$ V, 25 C
				400					nA		150 C
V_P	Gate-Source Pinch-Off Voltage		-5	-10	-2	-7	-1	-5	V	$V_{DS} = 20$ V, $I_D = 1$ nA	
I_{DSS}	Drain Current at Zero Gate Voltage		30		15		8		mA	$V_{DS} = 20$ V, $V_{GS} = 0$, Pulse-Test Duration = 2 ms	
$V_{DS(ON)}$	Drain-Source ON Voltage							0.2	V	$V_{GS} = 0$	$I_D = 2.5$ mA
						0.2					$I_D = 4$ mA
				0.2							$I_D = 6.6$ mA
$r_{DS(ON)}$	Static Drain-Source ON Resistance			30		50		80	Ω	$V_{GS} = 0$, $I_D = 1$ mA	
$r_{ds(on)}$	Small-Signal Drain-Source ON Resistance			30		50		80	Ω	$V_{GS} = 0$, $I_D = 0$, f = 1 kHz	
C_{iss}	Common-Source Input Capacitance			16		16		16	pF	$V_{DS} = 20$ V, $V_{GS} = 0$, f = 1 MHz	
		JAN TX Only		5		5		5	pF	$V_{DS} = 20$ V, $V_{GS} = 0$, f = 1 MHz	
C_{rss}	Common-Source Reverse Transfer Capacitance			5		5		5	pF	$V_{DS} = 0$, $V_{GS} = -20$ V, f = 1 MHz	

N-CHANNEL SILICON PLANAR EPITAXIAL J-FET

2N4117 2N4118 2N4119
2N4117A 2N4118A 2N4119A

FEATURES

- Low Leakage – $I_{GSS} < 1$ pA
- Low Capacitance – $C_{rss} < 1.5$ pF

GENERAL DESCRIPTION

Low leakage for low power avoid amplifiers.

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature TO72	-65°C to +200°C
Storage Temperature TO92	-65°C to +125°C
Operating Junction Temperature TO72	+200°C
Operating Junction Temperature TO92	+125°C
Lead Temperature (Soldering, 10 sec time limit)	300°C

Maximum Power Dissipation

Device Dissipation @ Free Air Temperature	300 mW
Linear Derating TO72	1.7 mW/°C
TO92	3.0 mW/°C

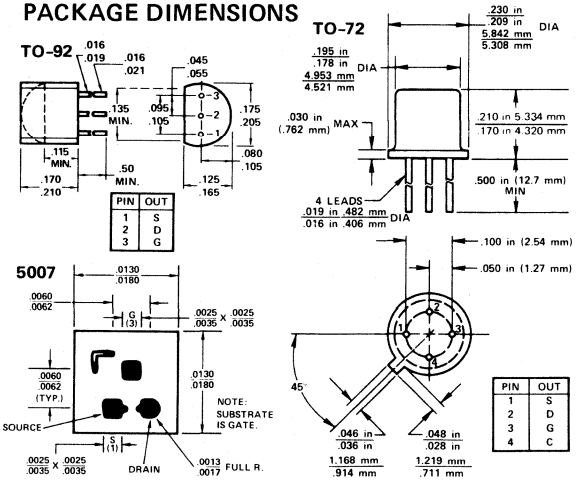
Maximum Voltages & Current

V_{GS} Gate to Source Voltage	-40 V
V_{GD} Gate to Drain Voltage	-40 V
I_G Gate Current	50 mA

ORDERING INFORMATION

TO72	TO92	WAFER	CHIP
2N4117	2N4117-TO92	2N4117/W	2N4117/D
2N4117A	2N4117A-TO92	2N4117A/W	2N4117A/D
2N4118	2N4118-TO92	2N4118/W	2N4118/D
2N4118A	2N4118A-TO92	2N4118A/W	2N4118A/D
2N4119	2N4119-TO92	2N4119/W	2N4119/D
2N4119A	2N4119A-TO92	2N4119A/W	2N4119A/D

PACKAGE DIMENSIONS



ELECTRICAL CHARACTERISTICS

(25°C unless otherwise noted)

PARAMETER		2N4117 2N4117A* MIN	2N4117 2N4117A* MAX	2N4118 2N4118A* MIN	2N4118 2N4118A* MAX	2N4119 2N4119A* MIN	2N4119 2N4119A* MAX	UNIT	TEST CONDITIONS
BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	$I_G = -1\ \mu A$, $V_{DS} = 0$
I_{GSS}	Gate Reverse Current		-10 -1*		-10 -1*		-10 -1*	pA	$V_{GS} = -20$ V, $V_{DS} = 0$
I_{GSS} (+150°C)	Gate Reverse Current		-25 -2.5*		-25 -2.5*		-25 -2.5*	nA	$V_{GS} = -20$ V, $V_{DS} = 0$
V_{GS} (off)	Gate-Source Pinch-Off Voltage	-0.6	-1.8	-1	-3	-2	-6	V	$V_{DS} = 10$ V, $I_D = 1$ nA
I_{DSS}	Drain Current at Zero Gate Voltage (Note 1)	0.02	0.09	0.08	0.24	0.20	0.60	mA	$V_{DS} = 10$ V $V_{GS} = 0$
g_{fs}	Common-Source Forward Transconductance (Note 1)	70	210	80	250	100	330	μmho	$V_{DS} = 10$ V f = 1 kHz
g_{fs}	Common-Source Forward Transconductance	60		70		90		μmho	$V_{GS} = 0$, f = 30 MHz
g_{os}	Common-Source Output Conductance		3		5		10	μmho	$V_{DS} = 10$ V, $V_{GS} = 0$, f = 1 kHz
C_{iss}	Common-Source Input Capacitance		3		3		3	pF	$V_{DS} = 10$ V, $V_{GS} = 0$, f = 1 kHz
C_{rss}	Common-Source Reverse Transfer Capacitance		1.5		1.5		1.5	pF	$V_{DS} = 10$ V, $V_{GS} = 0$, f = 1 kHz

NOTE:

1. Pulse test: Pulse duration of 2 ms used during test.

Intersil

N-CHANNEL
SILICON PLANAR
EPITAXIAL J-FET

2N4220 2N4221 2N4222

FEATURES

- $C_{rss} < 2$ pF
- Moderately High Forward Transconductance

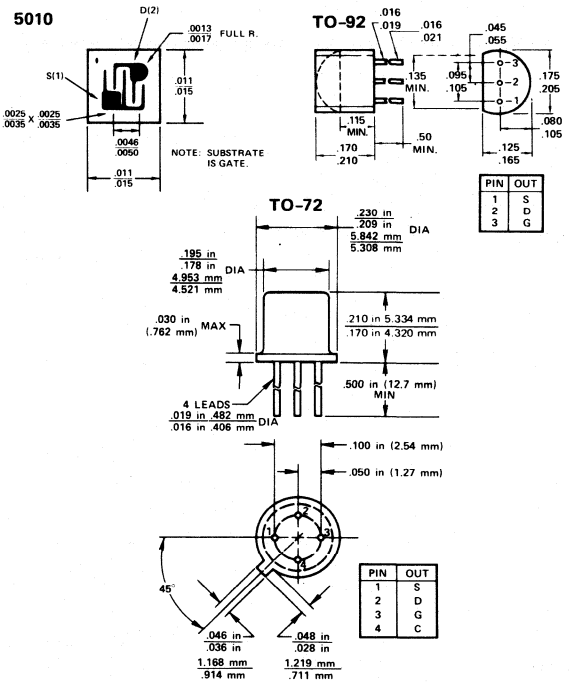
ORDERING INFORMATION

TO72	TO92	WAFER	CHIP
2N4220	2N4220-TO92	2N4220/W	2N4220/D
2N4221	2N4221-TO92	2N4221/W	2N4221/D
2N4222	2N4222-TO92	2N4222/W	2N4222/D

GENERAL DESCRIPTION

For small signal applications – UHF amplifier, oscillator and mixer applications.

PACKAGE DIMENSIONS



ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature TO72	−65°C to +200°C
Storage Temperature TO92	−55°C to +125°C
Operating Junction Temperature TO72	+200°C
Operating Junction Temperature TO92	+125°C
Lead Temperature (Soldering, 10 sec time limit)	+260°C

Maximum Power Dissipation

Device Dissipation @ Free Air Temperature	300 mW
Linear Derating TO72	1.7 mW/°C
TO92	3.0 mW/°C

Maximum Voltages & Current

V_{GS}	Gate to Source Voltage	−30 V
V_{GD}	Gate to Drain Voltage	−30 V
I_G	Gate Current	10 mA

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N4220 MIN	2N4220 MAX	2N4221 MIN	2N4221 MAX	2N4222 MIN	2N4222 MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		−0.1		−0.1		−0.1	nA	V_{GS} = −15 V, V_{DS} = 0	
			−0.1		−0.1		−0.1	μA		150°C
BV_{GSS}	Gate-Source Breakdown Voltage	−30		−30		−30		V	I_G = −10 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage		−4		−6		−8	V	V_{DS} = 15 V, I_D = 0.1 nA	
V_{GS}	Gate-Source Voltage	−0.5	−2.5	−1	−5	−2	−6	V	V_{DS} = 15 V, I_D = ( )	
		(50)	(50)	(200)	(200)	(500)	(500)	(μA)		
I_{DSS}	Saturation Drain Current (Note 3)	0.5	3	2	6	5	15	mA	V_{DS} = 15 V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance (Note 3)	1000	4000	2000	5000	2500	6000	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
$\lvert y_{fs} \rvert$	Common-Source Forward Transadmittance	750		750		750		μmho	V_{DS} = 15 V, V_{GS} = 0	f = 100 MHz
g_{os}	Common-Source Output Conductance (Note 3)		10		20		40	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
C_{iss}	Common-Source Input Capacitance		6		6		6	pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		2		2		2	pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz

Intersil

N-CHANNEL SILICON PLANAR EPITAXIAL J-FET

2N4223
2N4224

FEATURES

- NF = 3 dB Typical at 200 MHz
- $C_{rss} < 2$ pF

GENERAL DESCRIPTION

For VHF amplifier and mixer applications.

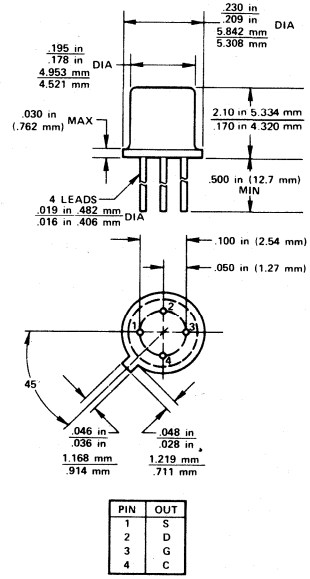
ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Gate-Drain or Gate-Source Voltage	-30 V
Gate Current	10 mA
Drain Current	20 mA
Total Device Dissipation at (or below) 25°C Free-Air Temperature	300 mW
Storage Temperature Range	-65°C to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

PACKAGE DIMENSIONS

TO-72



PIN	OUT
1	S
2	D
3	G
4	C

5000

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N4223 MIN	2N4223 MAX	2N4224 MIN	2N4224 MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		-0.25		-0.5	nA	V_{GS} = -20 V, V_{DS} = 0	
			-0.25		-0.5	μA		150°C
BV_{GSS}	Gate-Source Breakdown Voltage	-30		-30		V	I_G = -10 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.1	-8	-0.1	-8	V	V_{DS} = 15 V, I_D = ( )	
		(0.25)	(0.25)	(0.5)	(0.5)	(nA)		
V_{GS}	Gate-Source Voltage	-1.0	-7.0	-1.0	-7.5	V		
		(0.3)	(0.3)	(0.2)	(0.2)	(mA)		
I_{DSS}	Saturation Drain Current	3	18	2	20	mA	V_{DS} = 15 V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance	3000	7000	2000	7500	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
C_{iss}	Common-Source Input Capacitance (Output Shorted)		6		6	pF		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		2		2			
$\|Y_{fs}\|$	Common-Source Forward Transadmittance	2700		1700		μmho	V_{DS} = 15 V, V_{GS} = 0	f = 200 MHz
g_{iss}	Common-Source Input Conductance (Output Shorted)		800		800			
g_{oss}	Common-Source Output Conductance (Input Shorted)		200		200			
G_{ps}	Small Signal Power Gain	10				dB	V_{DS} = 15 V, V_{GS} = 0, R_{gen} = 1 K	
NF	Noise Figure		5					

Intersil

N-CHANNEL
SILICON PLANAR
EPITAXIAL J-FET

2N4338 2N4339
2N4340 2N4341

FEATURES

- Exceptionally high figure of merit
- Radiation Immunity
- Symmetrical devices for low-level choppers, data switches, multiplexers and low noise amplifiers
- Extremely low noise and capacitance
- High input impedance
- Zero offset
- High reliability silicon epitaxial planar construction

ORDERING INFORMATION

TO18	TO92	WAFER	CHIP
2N4338	2N4338-TO92	2N4338/W	2N4338/D
2N4339	2N4339-TO92	2N4339/W	2N4339/D
2N4340	2N4340-TO92	2N4340/W	2N4340/D
2N4341	2N4341-TO92	2N4341/W	2N4341/D

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature TO18	-65°C to +200°C
Storage Temperature TO92	-55°C to +125°C
Operating Junction Temperature TO18	+200°C
Operating Junction Temperature TO92	+125°C
Lead Temperature (Soldering, 10 sec time limit)	+260°C

Maximum Power Dissipation

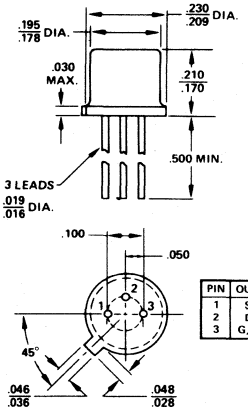
Device Dissipation @ Free Air Temperature	300 mW
Linear Derating TO18	1.7 mW/°C
TO92	3.0 mW/°C

Maximum Voltages & Current

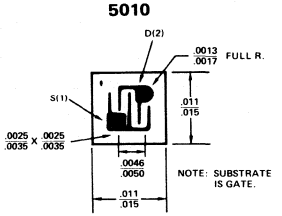
V_{GS} Gate to Source Voltage	-50 V
V_{GD} Gate to Drain Voltage	-50 V
I_G Gate Current	50 mA

PACKAGE DIMENSIONS

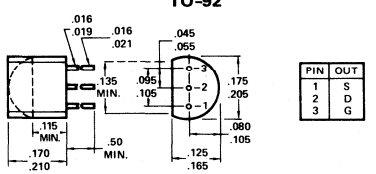
TO-18



5010



TO-92



ELECTRICAL CHARACTERISTICS (25°C unless otherwise specified)

PARAMETER		2N4338		2N4339		2N4340		2N4341		UNITS	TEST CONDITIONS	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
I_{GSS}	Gate Reverse Current		-0.1		-0.1		-0.1		-0.1	nA	V_{GS} = -30 V, V_{DS} = 0	
			-0.1		-0.1		-0.1		-0.1	μA		150°C
BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		-50		-50		V	I_G = -1 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.3	-1	-0.6	-1.8	-1	-3	-2	-6		V_{DS} = 15 V, I_D = 0.1 μA	
$I_{D(off)}$	Drain Cutoff Current		0.05 (-5)		0.05 (-5)		0.05 (-5)		0.07 (-10)	nA (V)	V_{DS} = 15 V, V_{GS} = ( )	
I_{DSS}	Saturation Drain Current (Note 3)	0.2	0.6	0.5	1.5	1.2	3.6	3	9	mA	V_{DS} = 15 V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance (Note 3)	600	1800	800	2400	1300	3000	2000	4000	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
g_{os}	Common-Source Output Conductance		5		15		30		60			
r_{ds}	Drain-Source ON Resistance		2500		1700		1500		800	ohm	V_{DS} = 0, V_{GS} = 0	
C_{iss}	Common-Source Input Capacitance		7		7		7		7	pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		3		3		3		3			
NF	Noise Figure		1		1		1		1	dB	V_{DS} = 15 V, V_{GS} = 0, R_{gen} = 1 meg, BW = 200 Hz	f = 1 kHz

Intersil

N-CHANNEL ENHANCEMENT MODE MOS FET

2N4351

FEATURES

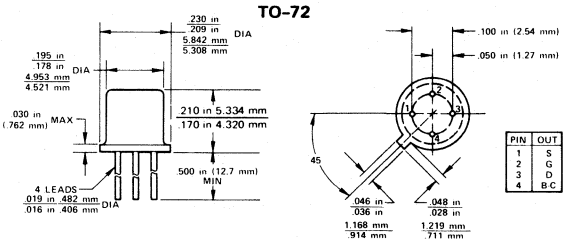
- Low On-Resistance – 50Ω
- Low Capacitance – 1.7 pF
- High Gain – 3,000 μmhos
- High Gate Breakdown Voltage – ±125 V
- Low Threshold Voltage – 3 V

ORDERING INFORMATION

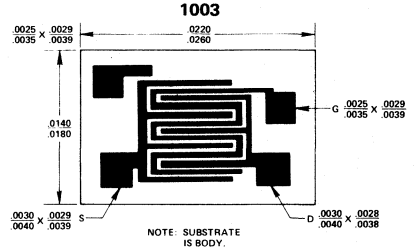
TO72	WAFER	CHIP
2N4351	2N4351/W	2N4351/D

PACKAGE DIMENSIONS

TO-72



1003



ABSOLUTE MAXIMUM RATINGS (Note 1)

@ 25°C (unless otherwise noted)

Maximum Temperatures

Operating Junction Temperature -55°C to +150°C

Maximum Power Dissipation

Total Dissipation at 25°C Ambient Temp 0.375 W

Linear Derating Factor at 25°C Ambient Temp. 3 mW/°C

Maximum Voltages and Current

V_{DSS} Drain to Source and Body Voltage 25 V

V_{GSS} Transient Gate to Source Voltage ±125 V

$I_{D(on)}$ Drain Current 100 mA

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Substrate connected to source.

PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS
OFF CHARACTERISTICS					
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	25		Vdc	I_D = 10 μA, V_{GS} = 0
I_{GSS}	Gate Leakage Current		10	pAdc	V_{GS} = ±30 Vdc, V_{DS} = 0
I_{DSS}	Zero-Gate-Voltage Drain Current		10	nAdc	V_{DS} = 10 V, V_{GS} = 0
ON CHARACTERISTICS					
$V_{GS(TH)}$	Gate-Source Threshold Voltage	1.0	5	Vdc	V_{DS} = 10 V, I_D = 10 μA
$I_{D(on)}$	"ON" Drain Current	3		mAdc	V_{GS} = 10 V, V_{DS} = 10 V
$V_{DS(on)}$	Drain-Source "ON" Voltage		1.0	Vdc	I_D = 2 mA, V_{GS} = 10 V
SMALL SIGNAL CHARACTERISTICS					
$r_{ds(on)}$	Drain-Source Resistance		300	ohms	V_{GS} = 10 V, I_D = 0, f = 1 kHz
$\|y_{fs}\|$	Forward Transfer Admittance	1000		μmho	V_{DS} = 10 V, I_D = 2 mA, f = 1 kHz
C_{rss}	Reverse Transfer Capacitance		1.3	pF	V_{DS} = 0, V_{GS} = 0, f = 140 kHz
C_{iss}	Input Capacitance		5.0	pF	V_{DS} = 10 V, V_{GS} = 0, f = 140 kHz
$C_{d(sub)}$	Drain-Substrate Capacitance		5.0	pF	$V_{D(SUB)}$ = 10 V, f = 140 kHz
SWITCHING CHARACTERISTICS					
t_{d1}	Turn-On Delay		45	ns	FIGURE 1 – SWITCHING CIRCUIT and WAVEFORMS
t_r	Rise Time		65	ns	
t_{d2}	Turn-Off Delay		60	ns	
t_f	Fall Time		100	ns	

FEATURES

- r_{ON} < 30 ohms (2N4391)
- $I_{D(off)}$ < 100 pA
- Switches ±10 VAC with ±15 V Supplies (2N4392, 2N4393)

Intersil

N–CHANNEL SILICON PLANAR EPITAXIAL J FET

2N4391 2N4392 2N4393

GENERAL DESCRIPTION

Most widely used solid state switching element. Generally require a translator circuit to boost logic levels up to ±15 V levels. Ideal for S & H circuits, R/2R ladder network and high frequency switching.

ORDERING INFORMATION

TO18	TO92	WAFER	CHIP
2N4391	2N4391-TO92	2N4391/W	2N4391/D
2N4392	2N4392-TO92	2N4392/W	2N4392/D
2N4393	2N4393-TO92	2N4393/W	2N4393/D

ABSOLUTE MAXIMUM RATINGS

@25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature TO18	−65°C to +200°C
Storage Temperature TO92	−55°C to +125°C
Operating Junction Temperature TO18	+200°C
Operating Junction Temperature TO92	+125°C
Lead Temperature (Soldering, 10 sec time limit)	+300°C

Maximum Power Dissipation

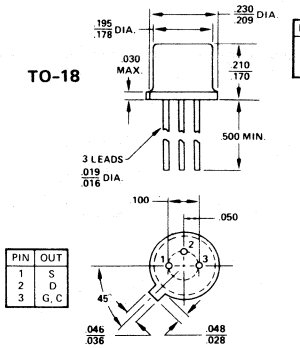
Device Dissipation @ Free Air Temperature	300 mW
Linear Derating TO18	1.7 mW/°C
TO92	3.0 mW/°C

Maximum Voltages & Current

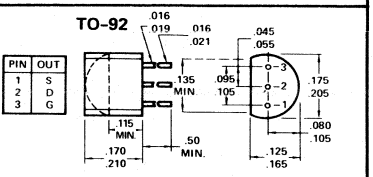
V_{GS}	Gate to Source Voltage	−40 V
V_{GD}	Gate to Drain Voltage	−40 V
I_G	Gate Current	50 mA

PACKAGE DIMENSIONS:

TO-18



TO-92



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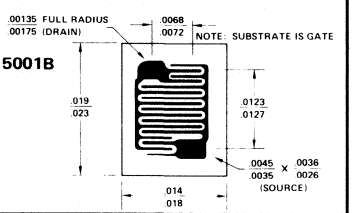
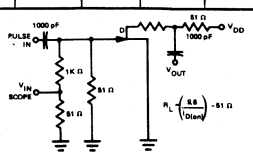


*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

CHARACTERISTIC		2N4391 MIN	2N4391 MAX	2N4392 MIN	2N4392 MAX	2N4393 MIN	2N4393 MAX	UNIT	TEST CONDITIONS		
I_{GSS}	Gate Reverse Current		−100		−100		−100	pA	V_{GS} = −20 V, V_{DS} = 0		
			−200		−200		−200	nA			150°C
BV_{GSS}	Gate-Source Breakdown Voltage	−40		−40		−40		V	I_G = 1 μA, V_{DS} = 0		
$I_{D(off)}$	Drain Cutoff Current						100	pA	V_{DS} = 20 V	V_{GS} = −5 V	
							200	nA			150°C
					100			pA		V_{GS} = −7 V	
					200			nA			150°C
			100					pA		V_{GS} = −12 V	
			200					nA			150°C
$V_{GS(f)}$	Gate-Source Forward Voltage		1		1		1	V	I_G = 1 mA, V_{DS} = 0		
$V_{GS(off)}$	Gate-Source Cutoff Voltage	−4	−10	−2	−5	−0.5	−3		V_{DS} = 20 V, I_D = 1 nA		
I_{DSS}	Saturation Drain Current (Note 1)	50	150	25	75	5	30	mA	V_{DS} = 20 V, V_{GS} = 0		
$V_{DS(on)}$	Drain Source ON Voltage						0.4	V	V_{GS} = 0	I_D = 3 mA	
					0.4					I_D = 6 mA	
			0.4							I_D = 12 mA	
$r_{DS(on)}$	Static Drain-Source ON Resistance		30		60		100	Ω	V_{GS} = 0, I_D = 1 mA		
$r_{ds(on)}$	Drain-Source ON Resistance		30		60		100	Ω	V_{GS} = 0, I_D = 0		f = 1 kHz
C_{iss}	Common-Source Input Capacitance		14		14		14	pF	V_{DS} = 20 V, V_{GS} = 0		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance						3.5		V_{DS} = 0	V_{GS} = −5 V	
					3.5					V_{GS} = −7 V	
			3.5							V_{GS} = −12 V	
t_d	Turn-ON Delay Time		15		15		15	ns	V_{DD} = 10 V, $V_{GS(on)}$ = 0		
t_r	Rise Time		5		5		5			$I_{D(on)}$	$V_{GS(off)}$
t_{off}	Turn-OFF Delay Time		20		35		50		2N4391	12 mA	−12 V
t_f	Fall Time		15		20		30		2N4392	6	−7
									2N4393	3	−5

NOTE:
1. Pulse test required, pulse width = 300 μs, duty cycle ≤ 3%



INPUT PULSE
RISE TIME < 0.5 ns
FALL TIME < 0.5 ns
PULSE DUTY CYCLE 1%

SAMPLING SCOPE
RISE TIME 0.4 ns
INPUT RESISTANCE 50 Ω

FEATURES

- Silicon Planar Epitaxial Construction
- Low Noise – NF = 2.0 dB max. @ 100 MHz
  NF = 4.0 dB max. @ 400 MHz
- Low Feedback Capacitance – C_{rss} = 0.8 pF max.
- Low Output Capacitance – C_{oss} = 2.0 pF max.
- High Transconductance – RE (Y_{fs}) = 4000 μmho min.
- High Power Gain – G_{ps} = 18 dB min. @ 100 MHz
  G_{ps} = 10 dB min. @ 400 MHz

Intersil

N-CHANNEL SILICON PLANAR EPITAXIAL J-FET

2N4416
2N4416A

GENERAL DESCRIPTION

For UHF amplifier and mixer applications

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature TO72	-65°C to +200°C
Storage Temperature TO92	-55°C to +125°C
Operating Junction Temperature TO72	+200°C
Operating Junction Temperature TO92	+125°C
Lead Temperature (Soldering, 10 sec time limit)	+300°C

Maximum Power Dissipation

Device Dissipation @ Free Air Temperature	300 mW
Linear Derating TO72	1.7 mW/°C
TO92	3.0 mW/°C

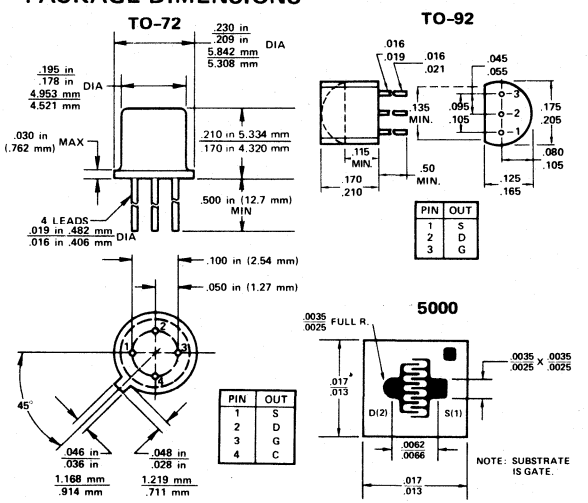
Maximum Voltages & Current

		2N4416	2N4416A
V_{GS}	Gate to Source Voltage	-30 V	-35 V
V_{GD}	Gate to Drain Voltage	-30 V	-35 V
I_G	Gate Current	10 mA	10 mA

ORDERING INFORMATION

TO92	TO92	WAFER	CHIP
2N4416	2N4416-TO92	2N4416/W	2N4416/D
2N4416A	2N4416A-TO92	2N4416A/W	2N4416A/D

PACKAGE DIMENSIONS



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		MIN	MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		-0.1	nA	V_{GS} = -20 V, V_{DS} = 0	
			-0.1	μA		150°C
BV_{GSS}	Gate-Source Breakdown Voltage	-30		V	I_G = -1 μA, V_{DS} = 0	2N4416
		-35				2N4416A
$V_{GS(off)}$	Gate-Source Cutoff Voltage		-6	V	V_{DS} = 15 V, I_D = 1 nA	2N4416
		-2.5	-6			2N4416A
I_{DSS}	Drain Current at Zero Gate Voltage	5	15	mA	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
g_{fs}	Common-Source Forward Transconductance	4500	7500	μmho		
g_{os}	Common-Source Output Conductance		50	μmho		
C_{rss}	Common-Source Reverse Transfer Capacitance		0.8	pF		f = 1 MHz
C_{iss}	Common-Source Input Capacitance		4	pF		
C_{oss}	Common-Source Output Capacitance		2			

PARAMETER		100 MHz MIN	100 MHz MAX	400 MHz MIN	400 MHz MAX	UNIT	TEST CONDITIONS
g_{iss}	Common-Source Input Conductance		100		1000	μmho	V_{DS} = 15 V, V_{GS} = 0
b_{iss}	Common-Source Input Susceptance		2500		10,000	μmho	
g_{oss}	Common-Source Output Conductance		75		100	μmho	
b_{oss}	Common-Source Output Susceptance		1000		4000	μmho	
g_{fs}	Common-Source Forward Transconductance			4000		μmho	
G_{ps}	Common-Source Power Gain	18		10		dB	V_{DS} = 15 V, I_D = 5 mA
NF	Noise Figure		2		4	dB	V_{DS} = 15 V, I_D = 5 mA, R_G = 1 KΩ

FEATURES

- $r_{DS(ON)} < 25\Omega$ (2N4856, 2N4859)
- $I_{D(off)} < 250$ pA
- Switches ±10 V Signals with ±15 V Supplies (2N4858, 2N4861)

Intersil

N–CHANNEL SILICON PLANAR EPITAXIAL J FET ANALOG SWITCHES

2N4856 thru 2N4861

GENERAL DESCRIPTION

For analog switches, commutators and choppers.

ABSOLUTE MAXIMUM RATINGS

@25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature TO18	−65°C to +200°C
Storage Temperature TO92	−55°C to +125°C
Operating Junction Temperature TO18	+200°C
Operating Junction Temperature TO92	+125°C
Lead Temperature (Soldering, 10 sec time limit)	+300°C

Maximum Power Dissipation

Device Dissipation @ Free Air Temperature	1.8w
Linear Derating TO18	10mW/°C
TO92	16mW/°C

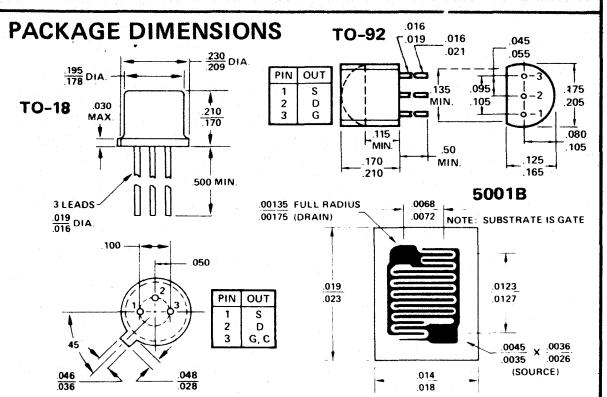
Maximum Voltages & Current

		2N4856-7-8	2N4859-60-61
V_{GS}	Gate to Source Voltage	−40 V	−30V
V_{GD}	Gate to Drain Voltage	−40 V	−30 V
I_G	Gate Current	50 mA	50 mA

ORDERING INFORMATION

TO18	TO92	WAFER	CHIP
2N4856	2N4856-TO92	2N4856/W	2N4856/D
2N4857	2N4857-TO92	2N4857/W	2N4857/D
2N4858	2N4858-TO92	2N4858/W	2N4858/D
2N4859	2N4859-TO92	2N4859/W	2N4859/D
2N4860	2N4860-TO92	2N4860/W	2N4860/D
2N4861	2N4861-TO92	2N4861/W	2N4861/D

PACKAGE DIMENSIONS

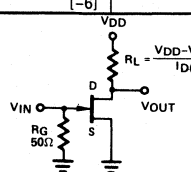


*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

CHARACTERISTIC			2N4856,59 MIN	2N4856,59 MAX	2N4857,60 MIN	2N4857,60 MAX	2N4858,61 MIN	2N4858,61 MAX	UNIT	TEST CONDITIONS	
BV_{GSS}	Gate-Source Breakdown Voltage	2N4856-58	−40		−40		−40		V	I_G = 1 μA, V_{DS} = 0	
		2N4859-61	−30		−30		−30				
I_{GSS}	Gate Reverse Current	2N4856-58		−250		−250		−250	pA	V_{GS} = −20 V, V_{DS} = 0	
		2N4859-61		−500		−500		−500	nA	V_{GS} = −15 V, V_{DS} = 0	150°C
$I_{D(off)}$	Drain Cutoff Current			250		250		250	pA	V_{DS} = 15 V, V_{GS} = −10 V	
				500		500		500	nA		150°C
$V_{GS(off)}$	Gate-Source Cutoff Voltage		−4	−10	−2	−6	−0.8	−4	V	V_{DS} = 15 V, I_D = 0.5 nA	
I_{DSS}	Saturation Drain Current (Note 1)		50		20	100	8	80	mA	V_{DS} = 15 V, V_{GS} = 0	
$V_{DS(on)}$	Drain-Source ON Voltage			0.75 (20)		0.50 (10)		0.50 (5)	V (mA)	V_{GS} = 0, I_D = ( )	
$r_{ds(on)}$	Drain-Source ON Resistance			25		40		60	ohm	V_{GS} = 0, I_D = 0	f = 1 kHz
C_{iss}	Common-Source Input Capacitance			18		18		18	pF	V_{DS} = 0, V_{GS} = −10 V	f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance			8		8		8			
t_d	Turn-ON Delay Time			6 (20) [−10]		6 (10) [−6]		10 (5) [−4]	ns (mA) [V]	V_{DD} = 10 V, R_L = 464 Ω 2N4856,59 / 953 Ω 2N4857,60 / 1910 Ω 2N4858,61; $V_{GS(on)}$ = 0; $I_{D(on)}$ = ( ), $V_{GS(off)}$ = ( )	
t_r	Rise Time			3 (20) [−10]		4 (10) [−6]		10 (5) [−4]	ns (mA) [V]		
t_{off}	Turn-OFF Time			25 (20) [−10]		50 (10) [−6]		100 (5) [−4]	ns (mA) [V]		

NOTE:

1. Pulse test required, pulsewidth = 100 μs, duty cycle ⩽ 10%.



INPUT PULSE
RISE TIME 0.25 ns
FALL TIME 0.75
PULSE WIDTH 100 ns
PULSE DUTY CYCLE < 10%

SAMPLING SCOPE
RISE TIME 0.75 ns
INPUT RESISTANCE 1 M
INPUT CAPACITANCE 2.5 pf

N-CHANNEL SILICON PLANAR EPITAXIAL J-FET

2N4867 2N4868 2N4869
2N4867A 2N4868A 2N4869A

FEATURES

- Lowest Noise Voltage – $e_n \leq 5$ nV/√Hz
- Low Leakage – $I_{GSS} \leq 0.25$ nA
- High Gain – $Y_{fs} \geq 1300 \leq 4000$ μmho

ORDERING INFORMATION

TO72	TO92	WAFER	CHIP
2N4867	2N4867-TO92	2N4867/W	2N4867/D
2N4867A	2N4867A-TO92	2N4867A/W	2N4867A/D
2N4868	2N4868-TO92	2N4868/W	2N4868/D
2N4868A	2N4868A-TO92	2N4868A/W	2N4868A/D
2N4869	2N4869-TO92	2N4869/W	2N4869/D
2N4869A	2N4869A-TO92	2N4869A/W	2N4869A/D

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature TO72	-65°C to +200°C
Storage Temperature TO92	-55°C to +125°C
Operating Junction Temperature TO72	+200°C
Operating Junction Temperature TO92	+125°C
Lead Temperature (Soldering, 10 sec time limit)	+260°C

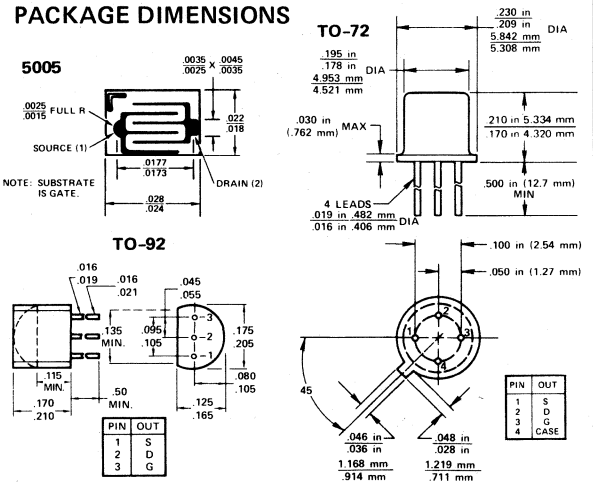
Maximum Power Dissipation

Device Dissipation @ Free Air Temperature	300 mW
Linear Derating TO72	1.7 mW/°C
TO92	3.0 mW/°C

Maximum Voltages & Current

V_{GS}	Gate to Source Voltage	-40 V
V_{GD}	Gate to Drain Voltage	-40 V
I_G	Gate Current	50 mA

PACKAGE DIMENSIONS



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N4867 2N4867A MIN	2N4867 2N4867A MAX	2N4868 2N4868A MIN	2N4868 2N4868A MAX	2N4869 2N4869A MIN	2N4869 2N4869A MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		-0.25 -0.25		-0.25 -0.25		-0.25 -0.25	nA μA	V_{GS} = -30 V, V_{DS} = 0	150°C
BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	I_G = -1 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.7	-2	-1	-3	-1.8	-5		V_{DS} = 20 V, I_D = 1 μA	
I_{DSS}	Saturation Drain Current (Note 1)	0.4	1.2	1	3	2.5	7.5	mA	V_{DS} = 20 V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance (Note 1)	700	2000	1000	3000	1300	4000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
g_{os}	Common-Source Output Conductance		1.5		4		10			
C_{rss}	Common-Source Reverse Transfer Capacitance		5		5		5	pF		f = 1 MHz
C_{iss}	Common-Source Input Capacitance		25		25		25			
$\bar{e}_n$	Short Circuit Equivalent Input Noise Voltage		20		20		20	nV/√Hz	V_{DS} = 10 V, V_{GS} = 0, 2N4867 Series	f = 10 Hz
			10		10		10		V_{DS} = 10 V, V_{GS} = 0, 2N4867A Series	
			10		10		10		V_{DS} = 10 V, V_{GS} = 0, 2N4867 Series	f = 1 kHz
			5		5		5		V_{DS} = 10 V, V_{GS} = 0, 2N4867A Series	
NF	Spot Noise Figure		1		1		1	dB	V_{DS} = 10 V, V_{GS} = 0, R_{gen} = 20 K, 2N4867 Series; 5 K, 2N4867A Series	f = 1 kHz

NOTE:

1. Pulse test duration = 2 ms.

FEATURES

- ON Resistance < 75 ohms on 2N5114
- $I_{D(off)}$ < 500 pA
- Switches directly from T^2L Logic (2N5116)

P–CHANNEL SILICON PLANAR EPITAXIAL J FET

2N5114 JAN TX 2N5114
2N5115 JAN TX 2N5115
2N5116 JAN TX 2N5116

GENERAL DESCRIPTION

Ideal for inverting switching or "Virtual Gnd" switching into inverting input of Op. Amp. No driver is required and ±10 VAC signals can be handled using only +5V logic (T^2L or CMOS).

ABSOLUTE MAXIMUM RATINGS

@25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature (TO18)	-65°C to +200°C
Storage Temperature (TO92)	-55°C to +125°C
Operating Junction Temperature (TO18)	+200°C
Operating Junction Temperature (TO92)	+125°C
Lead Temperature (Soldering, 10 sec time limit)	+260°C

Maximum Power Dissipation

Device Dissipation @ Free Air Temperature	500 mW
Linear Derating TO18	3.0 mW/°C
TO92	3.5 mW/°C

Maximum Voltages & Current

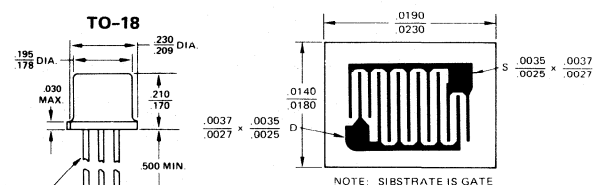
V_{GS}	Gate to Source Voltage	30 V
V_{GD}	Gate to Drain Voltage	30 V
I_G	Gate Current	50 mA

ORDERING INFORMATION

TO18	TO92	WAFER	CHIP
2N5114	2N5114-TO92	2N5114/W	2N5114/D
2N5115	2N5115-TO92	2N5115/W	2N5115/D
2N5116	2N5116-TO92	2N5116/W	2N5116/D
JAN TX 2N5114			
JAN TX 2N5115			
JAN TX 2N5116			

PACKAGE DIMENSIONS

5508B



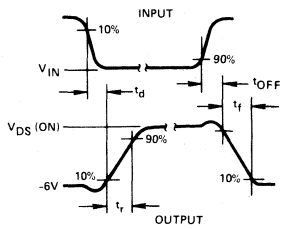
ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

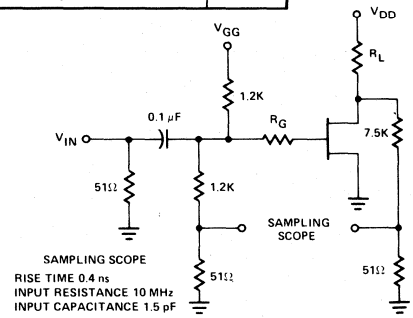
CHARACTERISTIC		2N5114 MIN	2N5114 MAX	2N5115 MIN	2N5115 MAX	2N5116 MIN	2N5116 MAX	UNIT	TEST CONDITIONS
BV_{GSS}	Gate-Source Breakdown Voltage	30		30		30		V	I_G = 1 μA, V_{DS} = 0
I_{GSS}	Gate Reverse Current		500		500		500	pA	V_{GS} = 20 V, V_{DS} = 0, 25°C
			1.0		1.0		1.0	μA	V_{GS} = 20 V, V_{DS} = 0, 150°C
$I_{D(OFF)}$	Drain Cutoff Current		-500		-500		-500	pA	V_{DS} = -15 V, V_{GS} = 2N5114 = 12 V, 2N5115 = 7 V, 2N5116 = 5 V, 25°C
			-1.0		-1.0		-1.0	μA	V_{DS} = -15 V, V_{GS} = 2N5114 = 12 V, 2N5115 = 7 V, 2N5116 = 5 V, 150°C
V_P	Gate-Source Pinch-Off Voltage	5	10	3	6	1	4	V	V_{DS} = -15 V, I_D = -1 nA
I_{DSS}	Drain Current at Zero Gate Voltage	-30	-90	-15	-60	-5	-25	mA	V_{GS} = 0, V_{DS} = 2N5114 = -18 V, 2N5115 = -15 V, 2N5116 = -15 V
$V_{GS(f)}$	Forward Gate-Source Voltage		-1		-1		-1	V	Pulse Test Duration = 2 ms, I_G = -1 mA, V_{DS} = 0
$V_{DS(ON)}$	Drain-Source ON Voltage		-1.3		-0.8		-0.6	V	V_{GS} = 0, I_D = 2N5114 = -15 mA, 2N5115 = - 7 mA, 2N5116 = - 3 mA
$R_{DS(ON)}$	Static Drain-Source ON Resistance		75		100		100	Ω	V_{GS} = 0, I_D = -1 mA
$r_{ds(ON)}$	Small-Signal Drain-Source ON Resistance		75		100		150	Ω	V_{GS} = 0, I_D = 0, f = 1 kHz
	Jan TX only		75		100		175	Ω	
C_{iss}	Common-Source Input Capacitance		25		25		25	pF	V_{DS} = -15 V, V_{GS} = 0, f = 1 MHz
	Jan TX only		25		25		27	pF	
C_{rss}	Common-Source Reverse Transfer Capacitance		7		7		7	pF	V_{DS} = 0, V_{GS} = 2N5114 = 12 V, 2N5115 = 7 V, 2N5116 = 5 V, f = 1 MHz

SWITCHING CHARACTERISTICS (@ 25°C unless otherwise noted)

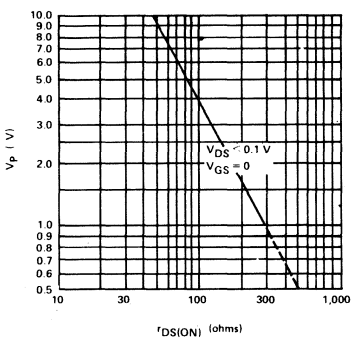
CHARACTERISTIC	2N5114	2N5115	2N5116	JAN TX 2N5114	JAN TX 2N5115	JAN TX 2N5116	UNIT
	MAX	MAX	MAX	MAX	MAX	MAX	
t_d Turn-ON Delay Time	6	10	12	6	10	25	ns
t_r Rise Time	10	20	30	10	20	35	ns
t_{off} Turn-OFF Delay Time	6	8	10	6	8	20	ns
t_f Fall Time	15	30	50	(not JAN TX specified)			ns

TEST CONDITIONS			
	2N5114	2N5115	2N5116
V_{DD}	-10 V	-6 V	-6 V
V_{GG}	20 V	12 V	8 V
R_L	430 Ω	910 Ω	2 KΩ
R_G	100 Ω	220 Ω	390 Ω
$I_{D(ON)}$	-15 mA	-7 mA	-3 mA
V_{IN}	-12 V	-7 V	-5 V

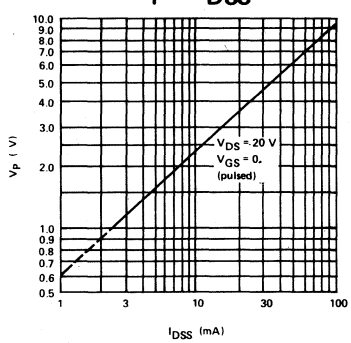




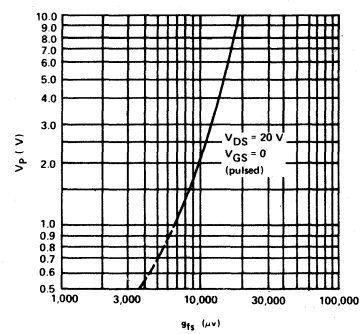
V_P vs $R_{DS(ON)}$



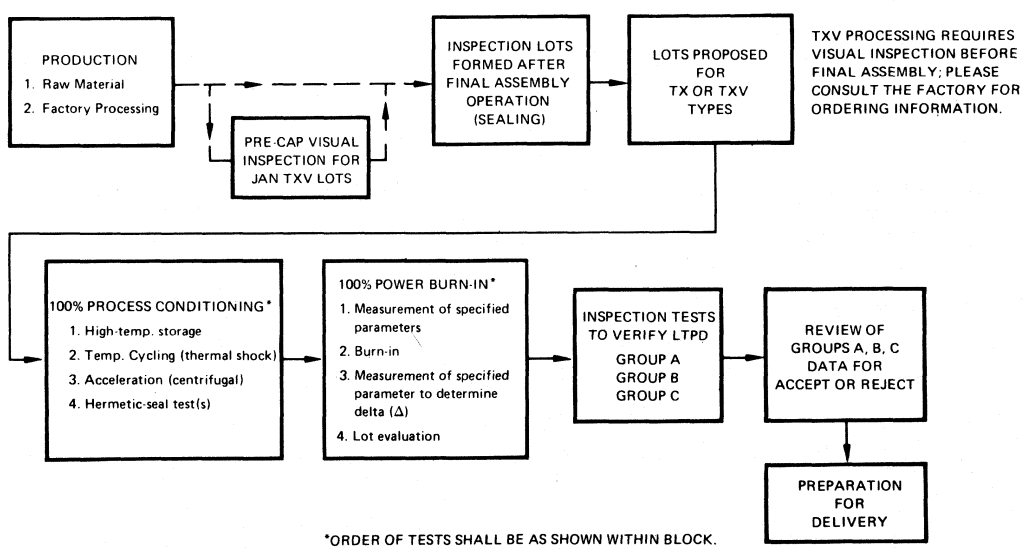
V_P vs I_{DSS}



V_P vs g_{fs}



TAN TX and JAN TX V Processing



GENERAL DESCRIPTION

Dielectrically isolated matched pairs for differential amplifiers.

MAXIMUM RATINGS (Note 1)
@ 25°C (unless otherwise noted)

Intersil

DUAL MONOLITHIC MATCHED PNP SILICON PLANAR TRANSISTORS

2N5117 2N5118 2N5119

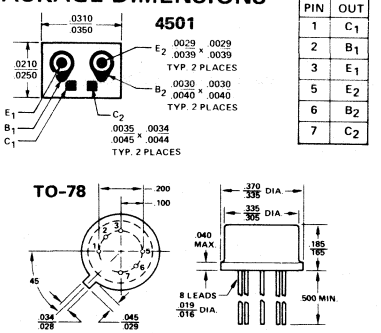
MAXIMUM RATINGS (25°C unless otherwise noted) (Note 1)

CHARACTERISTICS	SYMBOL	2N5117 2N5118 2N5119	UNITS
Dissipation at 25°C Case Temperature			
Each side (Note 1)	P_D	0.4	Watt
Both sides	P_D	0.75	Watt
Derating Factor			
Each side		2.3	mW/°C
Both sides		4.3	mW/°C
Voltage			
Collector to Base	V_{CBO}	45	Volts
Collector to Emitter	V_{CEO}	45	Volts
Emitter to Base (Note 2)	V_{EBO}	7.0	Volts
Collector to Collector	V_{CCO}	100	Volts
Collector Current	I_C	10	mA
Storage Temperature	T_S	-65 to +200	°C
Lead Temperature for 10 Seconds		+300	°C

ORDERING INFORMATION

TO78	WAFER	CHIP
2N5117	2N5117/W	2N5117/D
2N5118	2N5118/W	2N5118/D
2N5119	2N5119/W	2N5119/D

PACKAGE DIMENSIONS



PIN	OUT
1	C_1
2	B_1
3	E_1
5	E_2
6	B_2
7	C_2

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N5117 2N5118 MIN	2N5117 2N5118 MAX	2N5119 MIN	2N5119 MAX	UNIT	TEST CONDITIONS	
h_{FE}	DC Current Gain	100	300	50			I_C = 10 μA, V_{CE} = 5.0 V	
h_{FE}	DC Current Gain	100		50			I_C = 500 μA, V_{CE} = 5.0 V	
h_{FE}	DC Current Gain (-55°C)	30		20			I_C = 10 μA, V_{CE} = 5.0 V	
I_{CBO}	Collector Cutoff Current		0.1		0.1	nA	I_E = 0, V_{CB} = 30 V	
I_{CBO}	Collector Cutoff Current (150°C)		0.1		0.1	μA	I_E = 0, V_{CB} = 30 V	
I_{EBO}	Emitter Cutoff Current		0.1		0.1	nA	I_C = 0, V_{EB} = 5.0 V	
$I_{C1, C2}$	Collector-Collector Leakage		5.0		5.0	pA	V_{CC} = 100 V	
f_T	Current Gain Bandwith Product	100		100		MHz	I_C = 500 μA, V_{CE} = 10 V	
C_{ob}	Output Capacitance		0.8		0.8	pF	I_E = 0, V_{CB} = 5.0 V	
C_{TE}	Emitter Transition Capacitance		1.0		1.0	pF	I_C = 0, V_{EB} = 0.5 V	
$C_{C1, C2}$	Collector-Collector Capacitance		0.8		0.8	pF	V_{CC} = 0	
$V_{CEO(sust)}$	Collector-Emitter Sustaining Voltage	45		45		V	I_C = 1.0 mA, I_B = 0	
NF	Narrow Band Noise Figure		4.0		4.0	dB	I_C = 10 μA, V_{CE} = 5.0 V BW = 200 cps	f = 1 KHz, R_G = 10 KΩ
$V_{(BR)CBO}$	Collector Base Breakdown Voltage	45		45		V	I_C = 10 μA, I_E = 0	
$V_{(BR)EBO}$	Emitter Base Breakdown Voltage	7.0		7.0		V	I_E = 10 μA, I_C = 0	

MATCHING CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N5117 MIN	2N5117 MAX	2N5118 MIN	2N5118 MAX	2N5119 MIN	2N5119 MAX	UNIT	TEST CONDITIONS	
h_{FE_1}/h_{FE_2}	DC Current Gain Ratio (Note 3)	0.9	1.0	0.85	1.0	0.8	1.0		I_C = 10 μA to 500 μA, V_{CE} = 5 V I_C = 10 μA, V_{CE} = 5.0 V	
$V_{BE_1}-V_{BE_2}$	Base-Emitter Voltage Differential		3.0		5.0		5.0	mV	I_C = 10 μA to 500 μA, V_{CE} = 5 V I_C = 10 μA, V_{CE} = 5.0 V	
$I_{B_1}-I_{B_2}$	Base Current Differential		10.0		15		40	nA	I_C = 10 μA, V_{CE} = 5.0 V	
$\Delta(V_{BE_1}-V_{BE_2})$	Base Voltage Differential Change with Temperature		3.0		5.0		10	μV/°C	I_C = 10 μA, V_{CE} = 5.0 V	T_A = -55°C to +125°C
$\Delta(I_{B_1}-I_{B_2})$	Base-Current Differential Change with Temperature		0.3		0.5		1.0	nA/°C	I_C = 10 μA, V_{CE} = 5.0 V	T_A = -55°C to +125°C

1. Maximum ratings are limiting values above which devices may be damaged. These ratings give a maximum junction temperature of 200 C.
2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed 10 μA.
3. Lower of two h_{FE} readings is defined as h_{FE_1}.

LOW NOISE
MONOLITHIC DUAL
MATCHED N-CHANNEL
J-FETS (PAIR)

2N5196 2N5197 2N5198 2N5199

ABSOLUTE MAXIMUM RATINGS (Note 1)

@ 25°C (unless otherwise noted)

Maximum Temperatures
- Storage Temperature: -65°C to +200°C
- Operating Junction Temperature: +150°C
- Lead Temperature (Soldering, 10 sec. time limit): +300°C

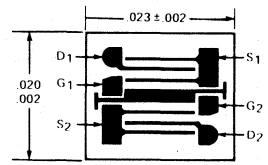
Maximum Power Dissipation
- Device Dissipation @ 85°C Free Air Temperature
  - One Side: 250 mW
  - Both Sides: 500 mW
- Linear Derating
  - One Side: 2.56 mW/°C
  - Both Sides: 4.3 mW/°C

Maximum Voltages & Currents
- V_{GS} Gate to Source Voltage: -50 V
- V_{GD} Gate to Drain Voltage: -50 V
- I_G Gate Current: 50 mA

ORDERING INFORMATION

TO71	WAFER	CHIP
2N5196	2N5196/W	2N5196/D
2N5197	2N5197/W	2N5197/D
2N5198	2N5198/W	2N5198/D
2N5199	2N5199/W	2N5199/D

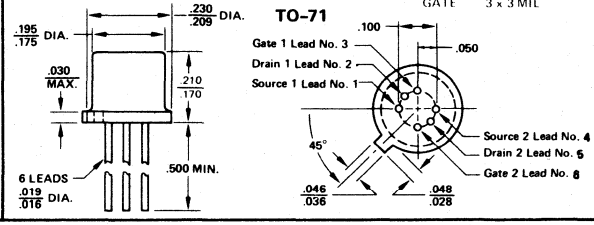
5017



SOURCE 3 x 6 MIL
DRAIN 3 x 3 MIL
GATE 3 x 3 MIL

PACKAGE DIMENSIONS

TO-71



ELECTRICAL CHARACTERISTICS (25°C unless otherwise specified)

PARAMETER		MIN	MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		-25	pA	V_{GS} = -30 V, V_{DS} = 0	
			-50	nA		150°C
BV_{GSS}	Gate-Source Breakdown Voltage	-50		V	I_G = -1 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.7	-4		V_{DS} = 20 V, I_D = 1 nA	
V_{GS}	Gate-Source Voltage	-0.2	-3.8			
I_G	Gate Operating Current		-15	pA	V_{DG} = 20 V, I_D = 200 μA	
			-15	nA		125°C
I_{DSS}	Saturation Drain Current (Note 1)	0.7	7	mA	V_{DS} = 20 V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance (Note 1)	1000	4000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
g_{fs}	Common-Source Forward Transconductance (Note 1)	700	1500		V_{DG} = 20 V, I_D = 200 μA	
g_{os}	Common-Source Output Conductance		50		V_{DS} = 20 V, V_{GS} = 0	
g_{os}	Common-Source Output Conductance		4		V_{DG} = 20 V, I_D = 200 μA	
C_{iss}	Common-Source Input Capacitance		6	pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		2			
NF	Spot Noise Figure		0.5	dB		f = 100 Hz, R_G = 10 MΩ
$\overline{e_n}$	Equivalent Input Noise Voltage		0.020	$\frac{\mu}{\sqrt{Hz}}$		f = 1 kHz
			20			

PARAMETER		2N5196 MIN	2N5196 MAX	2N5197 MIN	2N5197 MAX	2N5198 MIN	2N5198 MAX	2N5199 MIN	2N5199 MAX	UNIT	TEST CONDITIONS	
$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		5		5		5		5	nA	V_{DG} = 20 V, I_D = 200 μA	125°C
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Note 1)	0.95	1	0.95	1	0.95	1	0.95	1	—	V_{DS} = 20 V, V_{GS} = 0 V	
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 1)	0.97	1	0.97	1	0.95	1	0.95	1	—	V_{DG} = 20 V, I_D = 200 μA	f = 1 kHz
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		5		10		15	mV		
$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Differential Voltage Change with Temperature (Note 2)		5		10		20		40	μV/°C		T_A = 25°C, T_B = 125°C
			5		10		20		40			T_A = -55°C, T_B = 25°C
$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		1		1		1		1	μmho		f = 1 kHz

NOTES:
1. Pulse test required, pulsewidth = 300 μs, duty cycle ≤ 3%.
2. Measured at end points, T_A and T_B.

GENERAL DESCRIPTION

P-Channel junction depletion mode (Type A) field-effect transistors designed for general-purpose amplifier applications.

Intersil

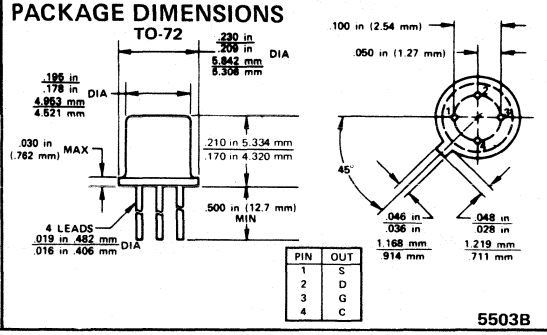
P-CHANNEL
SILICON PLANAR
EPITAXIAL J-FET

2N5265 thru 2N5270

MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{DS}	Drain-Source Voltage	60	Vdc
V_{DG}	Drain-Gate Voltage	60	Vdc
$V_{GS(r)}$	Reverse Gate-Source Voltage	60	Vdc
I_D	Drain Current	20	mAdc
$I_{G(f)}$	Gate Current-Forward	10	mAdc
P_D	Total Device Dissipation @ $T_A = 25°C$	300	mW
	Derate above 25°C	2.0	mW/°C
T_{stg}	Storage Temperature Range	-65 to +200	°C
T_J	Operating Junction Temperature Range	-65 to +175	°C

PACKAGE DIMENSIONS



ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

PARAMETER		MIN	MAX	UNIT	TEST CONDITIONS	
OFF CHARACTERISTICS						
$V_{(BR)GSS}$	Gate-Source Breakdwon Voltage	60		Vdc	$I_G = 10\ \mu Adc$, $V_{DS} = 0$	
$V_{GS(off)}$	Gate-Source Cutoff Voltage		3.0	Vdc	$V_{DS} = 15$ Vdc, $I_D = 1.0\ \mu Adc$	2N5265, 2N5266
			6.0			2N5267, 2N5268
			8.0			2N5269, 2N5270
I_{GSS}	Gate Reverse Current		2.0	nAdc	$V_{GS} = 30$ Vdc, $V_{DS} = 0$	
			2.0	μAdc	$V_{GS} = 30$ Vdc, $V_{DS} = 0$, $T_A = 150°C$	
ON CHARACTERISTICS						
I_{DSS}	Zero-Gate Voltage Drain Current	0.5	1.0	mAdc	$V_{DS} = 15$ Vdc, $V_{GS} = 0$	2N5265
		0.8	1.6			2N5266
		1.5	3.0			2N5267
		2.5	5.0			2N5268
		4.0	8.0			2N5269
		7.0	14			2N5270
V_{GS}	Gate-Source Voltage	0.3	1.5	Vdc	$V_{DS} = 15$ Vdc, $I_D = 0.05$ mAdc	2N5265
		0.4	2.0		$V_{DS} = 15$ Vdc, $I_D = 0.08$ mAdc	2N5266
		1.0	4.0		$V_{DS} = 15$ Vdc, $I_D = 0.15$ mAdc	2N5267
		1.0	4.0		$V_{DS} = 15$ Vdc, $I_D = 0.25$ mAdc	2N5268
		2.0	6.0		$V_{DS} = 15$ Vdc, $I_D = 0.4$ mAdc	2N5269
		2.0	6.0		$V_{DS} = 15$ Vdc, $I_D = 0.7$ mAdc	2N5270
SMALL-SIGNAL CHARACTERISTICS						
$\lvert y_{fs} \rvert$	Forward Transadmittance	900	2700	μmhos	$V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 1.0 kHz	2N5265
		1000	3000			2N5266
		1500	3500			2N5267
		2000	4000			2N5268
		2200	4500			2N5269
		2500	5000			2N5270
$Re(y_{is})$	Forward Transconductance	800		μmhos	$V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 100 MHz	2N5265
		900				2N5266
		1400				2N5267
		1700				2N5268
		1900				2N5269
		2100				2N5270
$\lvert y_{os} \rvert$	Output Admittance		75	μmhos	$V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 1.0 kHz	
C_{iss}	Input Capacitance		7.0	pF	$V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 1.0 MHz	
C_{rss}	Reverse Transfer Capacitance		2.0	pF	$V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 1.0 MHz	
NF	Common-Source Noise Figure		2.5	dB	$V_{DS} = 15$ Vdc, $V_{GS} = 0$, $R_G = 1.0$ M ohm, f = 100 Hz, BW = 1.0 Hz	
$\overline{e_n}$	Equivalent Short-Circuit Input Noise Voltage		115	nV/$\sqrt{Hz}$	$V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 100 Hz, BW = 1.0 Hz	

FEATURES

- G_{ps} = 10 dB Typical (Common Gate) at 450 MHz
- NF = 3.5 dB Typical at 450 MHz
- C_{rss} = 1 pF Typical

Intersil

N-CHANNEL SILICON PLANAR EPITAXIAL J-FET

2N5397
2N5398

GENERAL DESCRIPTION

For UHF amplifier, mixer and oscillator and video amplifier applications

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature TO72	-65°C to +200°C
Storage Temperature TO92	-55°C to +125°C
Operating Junction Temperature TO72	+200°C
Operating Junction Temperature TO92	+125°C
Lead Temperature (Soldering, 10 sec time limit)	300°C

Maximum Power Dissipation

Device Dissipation @ Free Air Temperature	300 mW
Linear Derating TO72	1.7 mW/°C
TO92	3.0 mW/°C

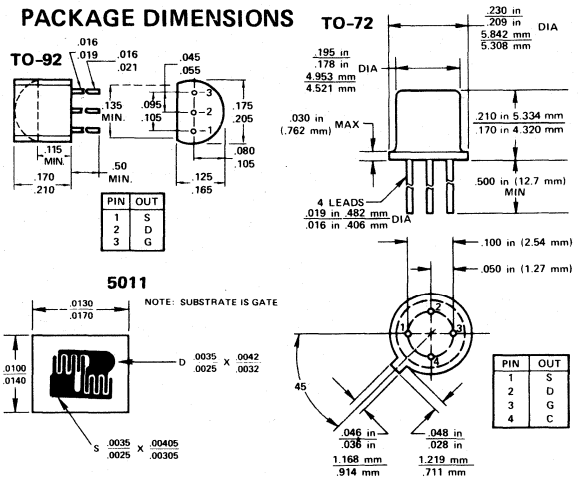
Maximum Voltages & Current

V_{GS} Gate to Source Voltage	-25 V
V_{GD} Gate to Drain Voltage	-25 V
I_G Gate Current	10 mA

ORDERING INFORMATION

TO72	TO92	WAFER	CHIP
2N5397	2N5397-TO92	2N5397/W	2N5397/D

PACKAGE DIMENSIONS



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N5397 MIN	2N5397 MAX	2N5398 MIN	2N5398 MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		-0.1		-0.1	nA	V_{GS} = -15 V, V_{DS} = 0	
			-0.1		-0.1	μA		150°C
BV_{GSS}	Gate-Source Breakdown Voltage	-25		-25		V	V_{DS} = 0, I_G = -1 μA	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1.0	-6.0	-1.0	-6.0		V_{DS} = 10 V, I_D = 1 nA	
I_{DSS}	Saturation Drain Current	10	30	5	40	mA	V_{DS} = 10 V, V_{GS} = 0	
$V_{GS(f)}$	Gate-Source Forward Voltage		1		1	V	V_{DS} = 0, I_G = 1 mA	
g_{fs}	Common-Source Forward Transconductance (Note 1)	6000	10,000			μmho	V_{DS} = 10V, I_D = 10 mA	f = 1 kHz
				5500	10,000		V_{DS} = 10 V, V_{GS} = 0	
g_{oss}	Common-Source Output Conductance		200				V_{DS} = 10 V, I_D = 10 mA	
					400		V_{DS} = 10 V, V_{GS} = 0	
C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			pF	V_{DS} = 10 V, I_D = 10 mA	f = 1 MHz
					1.3		V_{DS} = 10 V, V_{GS} = 0	
C_{iss}	Common-Source Input Capacitance		5.0				V_{DG} = 10 V, I_D = 10 mA	
					5.5		V_{DS} = 10 V, V_{GS} = 0	
g_{iss}	Common-Source Input Conductance		2000			μmho	V_{DG} = 10 V, I_D = 10 mA	f = 450 MHz
					3000		V_{DS} = 10 V, V_{GS} = 0	
g_{oss}	Common-Source Output Conductance		400				V_{DG} = 10 V, I_D = 10 mA	
					500		V_{DS} = 10 V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance **(Note 1)**	5500	9000				V_{DG} = 10 V, I_D = 10 mA	
				5000	10,000		V_{DS} = 10 V, V_{GS} = 0	
G_{ps}	Common-Source Power Gain (neutralized)	15				dB	V_{DG} = 10 V, I_D = 10 mA	
NF	Common-Source, Spot Noise Figure (neutralized)		3.5					

Note 1: **Pulse test duration = 2ms**

FEATURES

- Very Low Ron – $r_{DS} < 5$ ohms
- Excellent Switching – Turn-On < 4 ns
  Turn-Off < 6 ns
- Low Cutoff Current – $I_{D(off)} < 200$ pA

Intersil

N–CHANNEL
SILICON PLANAR
EPITAXIAL J FET

2N5432 2N5433 2N5434

GENERAL DESCRIPTION

Lowest Ron for analog switches, commutators and choppers

ORDERING INFORMATION

TO52	TO92	WAFER	CHIP
2N5432	2N5432-TO92	2N5432/W	2N5432/D
2N5433	2N5433-TO92	2N5433/W	2N5433/D
2N5434	2N5434-TO92	2N5434/W	2N5434/D

ABSOLUTE MAXIMUM RATINGS

@25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature TO52	-65°C to +200°C
Storage Temperature TO92	-55°C to +125°C
Operating Junction Temperature TO52	+200°C
Operating Junction Temperature TO92	+125°C
Lead Temperature (Soldering, 10 sec time limit)	+260°C

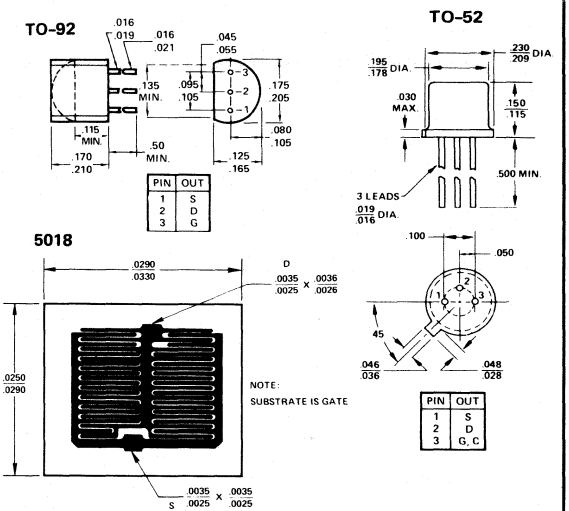
Maximum Power Dissipation

Device Dissipation @ Free Air Temperature	300 mW
Linear Derating TO52	2.3 mW/°C
TO92	4.8 mW/°C

Maximum Voltages & Current

V_{GS}	Gate to Source Voltage	-25 V
V_{GD}	Gate to Drain Voltage	-25 V
I_G	Gate Current	100 mA
I_D	Drain Current	400 mA

PACKAGE DIMENSIONS

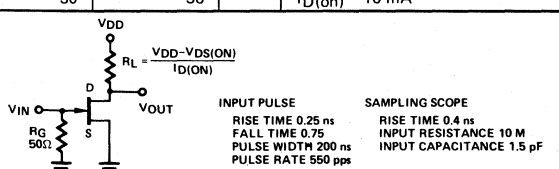


*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

CHARACTERISTIC		2N5432 MIN	2N5432 MAX	2N5433 MIN	2N5433 MAX	2N5434 MIN	2N5434 MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		-200		-200		-200	pA	V_{GS} = -15 V, V_{DS} = 0	
			-200		-200		-200	nA		150°C
BV_{GSS}	Gate Source Breakdown Voltage	-25		-25		-25		V	I_G = -1 μA, V_{DS} = 0	
$I_{D(off)}$	Drain Cutoff Current		200		200		200	pA	V_{DS} = 5 V, V_{GS} = -10 V	
			200		200		200	nA		150°C
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-4	-10	-3	-9	-1	-4	V	V_{DS} = 5 V, I_D = 3 nA	
I_{DSS}	Saturation Drain Current (Note 1)	150		100		30		mA	V_{DS} = 15 V, V_{GS} = 0	
$r_{DS(on)}$	Static Drain-Source ON Resistance	2	5		7		10	ohm	V_{GS} = 0, I_D = 10 mA	
$V_{DS(on)}$	Drain-Source ON Voltage		50		70		100	mV		
$r_{ds(on)}$	Drain-Source ON Resistance		5		7		10	ohm	V_{GS} = 0, I_D = 0	f = 1 kHz
C_{iss}	Common-Source Input Capacitance		30		30		30	pF	V_{DS} = 0, V_{GS} = -10 V	f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		15		15		15			
t_d	Turn-ON Delay Time		4		4		4	ns	V_{DD} = 1.5 V, $V_{GS(on)}$ = 0, $V_{GS(off)}$ = -12 V, $I_{D(on)}$ = 10 mA	
t_r	Rise Time		1		1		1			
t_{off}	Turn-OFF Delay Time		6		6		6			
t_f	Fall Time		30		30		30			

NOTE:

1. Pulse test required pulsewidth 300 μs, duty cycle ≤ 3%.



FEATURES

- Offset Voltage 5 mV
- Drift 5 $\mu V/^{\circ}C$
- Low Capacitance
- Low Output Conductance — 1 μmho Max

MONOLITHIC DUAL MATCHED N-CHANNEL J-FETS (PAIR)

2N5452 2N5453 2N5454

GENERAL DESCRIPTION

Matched FET pairs for differential amplifiers. This family of general purpose FETs is characterized for low and medium frequency differential amplifier applications requiring low drift and low offset voltage.

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	-65°C to +200°C
Operating Junction Temperature	+150°C
Lead Temperature (Soldering, 10 sec. time limit)	+300°C

Maximum Power Dissipation

Device Dissipation @ 85°C Free Air Temperature

One Side	250 mW
Both Sides	500 mW

Linear Derating

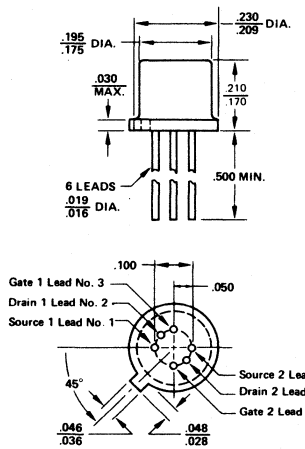
One Side	2.86 mW/°C
Both Sides	4.3 mW/°C

Maximum Voltages & Currents

V_{GS} Gate to Source Voltage	-50 V
V_{GD} Gate to Drain Voltage	-50 V

PACKAGE DIMENSIONS

TO-71



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ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	PARAMETER	2N5452 MIN	2N5452 MAX	2N5453 MIN	2N5453 MAX	2N5454 MIN	2N5454 MAX	UNITS	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		-100		-100		-100	pA	V_{GS} = -30 V, V_{DS} = 0	
			-200		-200		-200	nA		T_A = 150°C
BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		-50		V	V_{DS} = 0, I_G = -1 μA	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-4.5	-1	-4.5	-1	-4.5	V	V_{DS} = 20 V, I_D = 1 nA	
V_{GS}	Gate-Source Voltage	-0.2	-4.2	-0.2	-4.2	-0.2	-4.2	V	V_{DS} = 20 V, I_D = 50 μA	
$V_{GS(f)}$	Gate-Source Forward Voltage		2		2		2	V	V_{DS} = 0, I_G = 1 mA	
I_{DSS}	Saturation Drain Current	0.5	5.0	0.5	5.0	0.5	5.0	mA	V_{DS} = 20 V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance	1000	3000	1000	3000	1000	3000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
		1000		1000		1000				f = 100 MHz
g_{os}	Common-Source Output Conductance		3.0		3.0		3.0			f = 1 kHz
			1.0		1.0		1.0		V_{DS} = 20 V, I_D = 200 μA	
C_{iss}	Common-Source Input Capacitance		4.0		4.0		4.0	pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		1.2		1.2		1.2			
C_{dgo}	Drain-Gate Capacitance		1.5		1.5		1.5		V_{DG} = 10 V, I_S = 0	
$\overline{e_n}$	Equivalent Short Circuit Input Noise Voltage		20		20		20	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
NF	Common-Source Spot Noise Figure		0.5		0.5		0.5	dB	V_{DS} = 20 V, V_{GS} = 0, R_G = 10 MΩ	f = 100 Hz
I_{DSS1}/I_{DSS2}	Drain Saturation Current Ratio	0.95	1.0	0.95	1.0	0.95	1.0		V_{DS} = 20 V, V_{GS} = 0	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5.0		10.0		15.0	mV	V_{DS} = 20 V, I_D = 200 μA	
$\Delta\lvert V_{GS1}-V_{GS2}\rvert$	Gate-Source Voltage Differential Change with Temperature		0.4		0.8		2.0			T = 25°C to -55°C
			0.5		1.0		2.5			T = 25°C to +125°C
g_{fs1}/g_{fs2}	Transconductance Ratio	0.97	1.0	0.97	1.0	0.95	1.0			
$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		0.25		0.25		0.25	μmhos		f = 1 kHz

Intersil

N-CHANNEL
SILICON J-FET

2N5457 2N5458 2N5459

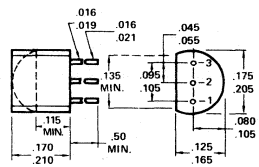
SMALL-SIGNAL AMPLIFIERS, CHOPPERS AND CONTROLLED RESISTORS

ABSOLUTE MAXIMUM RATINGS
(25°C unless otherwise noted)

SYMBOL	RATING	VALUE	UNIT
V_{DS}	Drain-Source Voltage	25	Vdc
V_{DG}	Drain-Gate Voltage	25	Vdc
$V_{GS(r)}$	Reverse Gate-Source Voltage	25	Vdc
I_G	Gate Current	10	mAdc
P_D	Total Device Dissipation @ T_A = 25°C Derate above 25°C	310 2.82	mW mW/°C
T_J	Operating Junction Temperature	135	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C

PACKAGE DIMENSIONS

TO-92



PIN	OUT
1	D
2	S
3	G

5010

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNITS	TEST CONDITIONS	
OFF CHARACTERISTICS							
BV_{GSS}	Gate-Source Breakdown Voltage	−25	−60		Vdc	I_G = −10 μAdc, V_{DS} = 0	
I_{GSS}	Gate Reverse Current		.05	−1.0 −200	nAdc	V_{GS} = −15 Vdc, V_{DS} = 0 V_{GS} = −15 Vdc, V_{DS} = 0, T_A = 100°C	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.5 −1.0 −2.0		−6.0 −7.0 −8.0	Vdc	V_{DS} = 15 Vdc, I_D = 10 nAdc	2N5457 2N5458 2N5459
V_{GS}	Gate-Source Voltage		2.5 3.5 4.5		Vdc	V_{DS} = 15 Vdc, I_D = 100 μAdc V_{DS} = 15 Vdc, I_D = 200 μAdc V_{DS} = 15 Vdc, I_D = 400 μAdc	2N5457 2N5458 2N5459
ON CHARACTERISTICS							
I_{DSS}	Zero-Gate-Voltage Drain Current	1.0 2.0 4.0	3.0 6.0 9.0	5.0 9.0 16	mAdc	V_{DS} = 15 Vdc, V_{GS} = 0	2N5457 2N5458 2N5459
DYNAMIC CHARACTERISTICS							
$\|y_{fs}\|$	Forward Transfer Admittance	1000 1500 2000	3000 4000 4500	5000 5500 6000	μmhos	V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 kHz	2N5457 2N5458 2N5459
$\|y_{os}\|$	Output Admittance		10	50	μmhos	V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 kHz	
C_{iss}	Input Capacitance		4.5	7.0	pF	V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 MHz	
C_{rss}	Reverse Transfer Capacitance		1.5	3.0	pF	V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 MHz	

Intersil

P-CHANNEL
SILICON PLANAR
EPITAXIAL J-FET

2N5460 thru 2N5465

MAXIMUM RATINGS

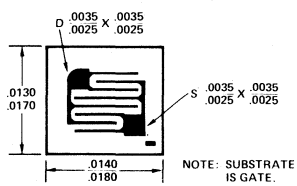
RATING	SYMBOL	2N5460 2N5461 2N5462	2N5463 2N5464 2N5465	UNITS
Drain-Gate Voltage	V_{DG}	40	60	Vdc
Reverse Gate-Source Voltage	$V_{GS(r)}$	40	60	Vdc
Forward Gate Current	$I_{G(f)}$	10		mAdc
Total Device Dissipation @ $T_A = 25°C$	P_D	310		mW
Derate above 25°C		2.82		mW/°C
Storage Temperature Range	T_{stg}	-65 to +150		°C
Operating Junction Temperature Range	T_J	-65 to +135		°C

ORDERING INFORMATION

TO92	WAFER	CHIP
2N5460	2N5460/W	2N5460/D
2N5461	2N5461/W	2N5461/D
2N5462	2N5462/W	2N5462/D
2N5463	2N5463/W	2N5463/D
2N5464	2N5464/W	2N5464/D
2N5465	2N5465/W	2N5465/D

PACKAGE DIMENSIONS

5503B



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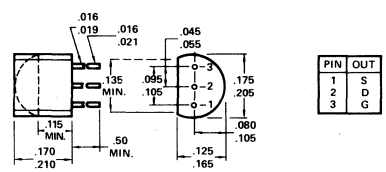


ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNITS	TEST CONDITIONS	
$V_{(BR)GSS}$	Gate-Source Breakdown Voltage	40 60			Vdc	$I_G = 10\ \mu Adc$, $V_{DS} = 0$	2N5460, 2N5461, 2N5462 2N5463, 2N5464, 2N5465
$V_{GS(off)}$	Gate-Source Cutoff Voltage	0.75 1.0 1.8		6.0 7.5 9.0	Vdc	$V_{DS} = 15$ Vdc, $I_D = 1.0\ \mu Adc$	2N5460, 2N5463 2N5461, 2N5464 2N5462, 2N5465
I_{GSS}	Gate Reverse Current			5.0 5.0 1.0 1.0	na na μAdc na	$V_{GS} = 20$ Vdc, $V_{DS} = 0$ $V_{GS} = 30$ Vdc, $V_{DS} = 0$ $V_{GS} = 20$ Vdc, $V_{DS} = 0$, $T_A = 100°C$ $V_{GS} = 30$ Vdc, $V_{DS} = 0$, $T_A = 100°C$	2N5460, 2N5461, 2N5462 2N5463, 2N5464, 2N5465 2N5460, 2N5461, 2N5462 2N5463, 2N5464, 2N5465
ON CHARACTERISTICS							
I_{DSS}	Zero-Gate Voltage Drain Current	1.0 2.0 4.0		5.0 9.0 16	mAdc	$V_{DS} = 15$ Vdc, $V_{GS} = 0$	2N5460, 2N5463 2N5461, 2N5464 2N5462, 2N5465
V_{GS}	Gate-Source Voltage	0.5 0.8 1.5		4.0 4.5 6.0	Vdc	$V_{DS} = 15$ Vdc, $I_D = 0.1$ mAdc $V_{DS} = 15$ Vdc, $I_D = 0.2$ mAdc $V_{DS} = 15$ Vdc, $I_D = 0.4$ mAdc	2N5460, 2N5463 2N5461, 2N5464 2N5462, 2N5465
SMALL-SIGNAL CHARACTERISTICS							
$\lvert g_{fs} \rvert$	Forward Transadmittance	1000 1500 2000		4000 5000 6000	μmhos	$V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 1.0 kHz	2N5460, 2N5463 2N5461, 2N5464 2N5462, 2N5465
g_{os}	Output Admittance			75	μmhos	$V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 1.0 kHz	
C_{iss}	Input Capacitance		5.0	7	pF	$V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 1.0 MHz	
C_{rss}	Reverse Transfer Capacitance		1.0	2.0	pF	$V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 1.0 MHz	
NF	Common-Source Noise Figure		1.0	2.5	dB	$V_{DS} = 15$ Vdc, $V_{GS} = 0$, $R_G = 1.0$ Megohm, f = 100 Hz, BW = 1.0 Hz	
$\overline{e_n}$	Equivalent Short-Circuit Input Noise Voltage		60	115	$nV/\sqrt{Hz}$	$V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 100 Hz, BW = 1.0 Hz	

Intersil

N-CHANNEL
SILICON PLANAR
EPITAXIAL J-FET

2N5484 2N5485 2N5486

GENERAL DESCRIPTION

For VHF/UHF amplifier, mixer and oscillator applications.

FEATURES

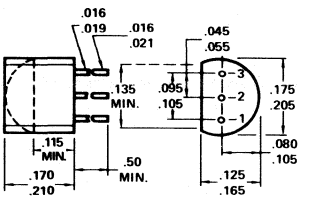
- Specified for 400 MHz Operation
- Can Be Used as a Low Capacitance Switch
- Economy Packaging
- $L_oC_{rss} < 1.0$ pF

ABSOLUTE MAXIMUM RATINGS

Drain-Gate Voltage	25 V
Source Gate Voltage	25 V
Drain Current	30 mA
Forward Gate Current	10 mA
Total Device Dissipation @ 25°C	310 mW
Derate above 25°C	2.82 mW/°C
Operating Junction Temperature Range	−65°C to +150°C
Storage Temperature Range	−65°C to +150°C

PACKAGE DIMENSIONS

TO-92



PIN	OUT
1	D
2	S
3	G

5000

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N5484		2N5485		2N5486		UNITS	TEST CONDITIONS	
		MIN	MAX	MIN	MAX	MIN	MAX			
I_{GSS}	Gate Reverse Current		−1.0		−1.0		−1.0	nA	V_{GS} = −20 V, V_{DS} = 0	
			−200		−200		−200			T_A = +100°C
BV_{GSS}	Gate-Source Breakdown Voltage	−25		−25		−25		V	I_G = −1 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.3	−3.0	−0.5	−4.0	−2.0	−6.0		V_{DS} = 15 V, I_D = 10 nA	
I_{DSS}	Saturation Drain Current	1.0	5.0	4.0	10	8.0	20	mA	V_{DS} = 15 V, V_{GS} = 0 (Note 1)	
g_{fs}	Common-Source Forward Transconductance	3000	6000	3500	7000	4000	8000	μmhos	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
g_{os}	Common-Source Output Conductance		50		60		75			
$Re_{(yfs)}$	Common-Source Forward Transconductance	2500								f = 100 MHz
				3000		3500				f = 400 MHz
$Re_{(yos)}$	Common-Source Output Conductance		75							f = 100 MHz
					100		100			f = 400 MHz
$Re_{(yis)}$	Common-Source Input Conductance		100							f = 100 MHz
					1000		1000			f = 400 MHz
C_{iss}	Common-Source Input Capacitance		5.0		5.0		5.0	pF		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		1.0		1.0		1.0			
C_{oss}	Common-Source Output Capacitance		2.0		2.0		2.0			
NF	Noise Figure		2.5		2.5		2.5	dB	V_{DS} = 15 V, V_{GS} = 0, R_G = 1 MΩ	f = 1 kHz
			3.0						V_{DS} = 15 V, I_D = 1 mA, R_G = 1 kΩ	f = 100 MHz
					2.0		2.0		V_{DS} = 15 V, I_D = 4 mA, R_G = 1 kΩ	f = 400 MHz
					4.0		4.0			
G_{ps}	Common-Source Power Gain	16	25						V_{DS} = 15 V, I_D = 1 mA	f = 100 MHz
				18	30	18	30		V_{DS} = 15 V, I_D = 4 mA	
				10	20	10	20			f = 400 MHz

GENERAL DESCRIPTION

Matched FET pairs for differential amplifiers.

MONOLITHIC DUAL
MATCHED N-CHANNEL
SILICON PLANAR
EPITAXIAL J-FETS (PAIR)

2N5515 thru 2N5524

ABSOLUTE MAXIMUM RATINGS (Note 1)

@25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	-65°C to +200°C

Maximum Power Dissipation	ONE SIDE	BOTH SIDES
Device Dissipation	250 mW	500 mW
@ Free Air Temperature	85°C	85°C
Linear Derating	3.85 mW/°C	7.7 mW/°C

Maximum Voltages & Current

V_{GS}	Gate to Source Voltage	-40 V
V_{GD}	Gate to Drain Voltage	-40 V
I_G	Gate Current	50 mA

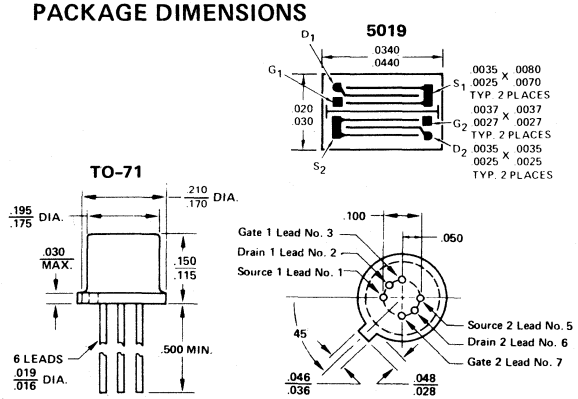
ORDERING INFORMATION

TO71	WAFER	CHIP
2N5515	2N5515/W	2N5515/D
2N5516	2N5516/W	2N5516/D
2N5517	2N5517/W	2N5517/D
2N5518	2N5518/W	2N5518/D
2N5519	2N5519/W	2N5519/D
2N5520	2N5520/W	2N5520/D
2N5521	2N5521/W	2N5521/D
2N5522	2N5522/W	2N5522/D
2N5523	2N5523/W	2N5523/D
2N5524	2N5524/W	2N5524/D

FEATURES

- Tight Temperature Tracking – $\Delta V_{GS} < 5\ \mu V/°C$
- Tight Matching –
  - $V_{GS} < 5$ mV
  - $I_G < 10$ nA @ 125°C
  - $g_{fs} < 3\%$
  - $g_{oss} < .1\ \mu$mho
- High Common Mode-Rejection – CMRR < 100 db
- Low Noise – $e_n < 15$ nV / $\sqrt{Hz}$ @10 Hz

PACKAGE DIMENSIONS



ELECTRICAL CHARACTERISTICS

(25°C unless otherwise noted)

PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current (+ 25°C)		-250	pA	V_{GS} = -30 V, V_{DS} = 0	
	(+150°C)		-250	nA		
BV_{GSS}	Gate-Source Breakdown Voltage	-40		V	I_G = 1 μA, V_{DS} = 0	
V_P	Gate-Source Pinch-Off Voltage	-0.7	-4	V	V_{DS} = 20 V, I_D = 1 nA	
I_{DSS}	Drain Current at Zero Gate Voltage (Note 2)	0.5	7.5	mA	V_{DS} = 20 V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance (Note 2)	1000	4000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
g_{oss}	Common-Source Output Conductance		10	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
C_{rss}	Common-Source Reverse Transfer Capacitance		5	pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
C_{iss}	Common-Source Input Capacitance		25	pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
$\bar{e}_n$	Equivalent Input Noise Voltage 2N5515-19		30	nV/$\sqrt{Hz}$	V_{DG} = 20 V, I_D = 200 μA	f = 10 Hz
	2N5520-24		15	nV/$\sqrt{Hz}$	V_{DG} = 20 V, I_D = 200 μA	f = 10 Hz
	2N5515-24		10	nV/$\sqrt{Hz}$	V_{DG} = 20 V, I_D = 200 μA	f = 1 kHz
I_G	Gate Current (+ 25°C)		-100	pA	V_{DG} = 20 V, I_D = 200 μA	
	(+125°C)		-100	nA		
V_{GS}	Gate Source Voltage	-0.2	-3.8	V	V_{DG} = 20 V, I_D = 200 μA	
g_{fs}	Common-Source Forward Transconductance (Note 2)	500	1000	μmho	V_{DG} = 20 V, I_D = 200 μA	f = 1 kHz
g_{oss}	Common-Source Output Conductance		1	μmho	V_{DG} = 20 V, I_D = 200 μA	

Additional Electrical Characteristics and Notes on Page 2.

MATCHING CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N5515,20		2N5516,21		2N5517,22		2N5518,23		2N5519,24		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
I_{DSS1}	Drain Current Ratio at	0.95	1	0.95	1.	0.95	1	0.95	1	0.90	1		V_{DS} = 20 V, V_{GS} = 0
I_{DSS2}	Zero Gate Voltage (Note 2)												
$\lvert I_{G1} - I_{G2} \rvert$	Differential Gate Current (+125°C)		10		10		10		10		10	nA	V_{DG} = 20 V, I_D = 200 μA
g_{fs1}	Transconductance Ratio	0.97	1	0.97	1	0.95	1	0.95	1	0.90	1		V_{DG} = 20 V, I_D = 200 μA
g_{fs2}	(Note 2)												f = 1 KHz
$\lvert g_{oss1} - g_{oss2} \rvert$	Differential Output Conductance		0.1		0.1		0.1		0.1		0.1	μmho	V_{DG} = 20 V, I_D = 200 μA f = 1 KHz
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage		5		5		10		15		15	mV	V_{DG} = 20 V, I_D = 200 μA
$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (T_A = +25°C to +125°C)		5		10		20		40		80	μV/°C	V_{DG} = 20 V, I_D = 200 μA
$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (T_A = +25 to -55°C)		5		10		20		40		80	μV/°C	V_{DG} = 20 V, I_D = 200 μA
CMRR	Common Mode Rejection Ratio (Note 3)	100		100		90						dB	V_{DD} = 10 to 20 V, I_D = 200 μA

NOTES:

1. These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
2. Pulse duration of 28mS used during test.
3. CMRR = $20\text{Log}_{10}\Delta V_{DD}/\Delta \lvert V_{GS1} - V_{GS2} \rvert$, ($\Delta V_{DD}$ = 10V)

FEATURES

- Good Combination of $r_{DS(on)}$ [< 150Ω] and Low C_{GS} Capacity (< 1.2 pF)

Intersil

N–CHANNEL SILICON PLANAR EPITAXIAL J FET

2N5555

GENERAL DESCRIPTION

Makes ideal sample and hold switch. Low G_{GS} gives very low charge injection; low $I_{D(off)}$ produces super low S & H drift rate. $V_{GS(off)}$ less than 5 V allows one to switch ±10 VAC with ±15 V supplies.

ABSOLUTE MAXIMUM RATINGS

@25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	-55°C to +125°C
Operating Junction Temperature @ Free Air Temperature	+125°C
Lead Temperature (Soldering, 10 second time limit)	+300°C

Maximum Power Dissipation

Device Dissipation	300 mW
Linear Derating	3.0 mW/°C

Maximum Voltages & Current

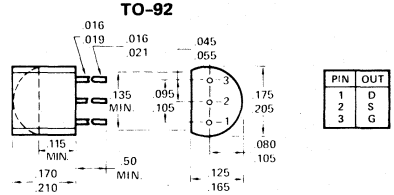
V_{SG} Source to Gate Voltage	25 V
V_{DS} Drain to Source Voltage	25 V
V_{DG} Drain to Gate Voltage	25 V
I_G Gate Current	10 mA

ORDERING INFORMATION

TO92	WAFER	CHIP
2N5555	2N5555/W	2N5555/D

PACKAGE DIMENSIONS

TO-92



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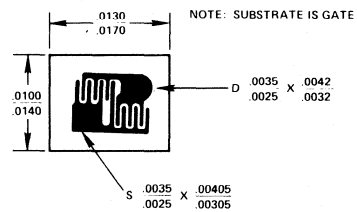


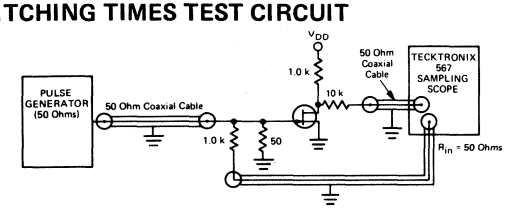
ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	TEST CONDITIONS
$V_{(BR)GSS}$	Gate-Source Breakdown Voltage	25	–	Vdc	I_G = 10 μAdc, V_{DS} = 0
I_{GSS}	Gate Reverse Current	–	1.0	nAdc	V_{GS} = 15 Vdc, V_{DS} = 0
$I_{D(off)}$	Drain Cutoff Current	–	100	pAdc	V_{DS} = 12 Vdc, V_{GS} = 10 Vdc
		–	2.0	μAdc	V_{DS} = 12 Vdc, V_{GS} = 10 Vdc, T_A = 100°C)
$V_{GS(off)}$	Gate-Source to Gate-Source Drain Cut-off Voltage	–	5	Vdc	@V_{DS} = 10 V, @ I_D = 1 nA
I_{DSS}	Zero-Gate Voltage Drain Current	15	–	mAdc	V_{DS} = 15 Vdc, V_{GS} = 0
$V_{GS(f)}$	Gate-Source Forward Voltage	–	1.0	Vdc	$I_{G(f)}$ = 1.0 mAdc, V_{DS} = 0
$V_{DS(on)}$	Drain-Source "ON" Voltage	–	1.5	Vdc	I_D = 7.0 mAdc, V_{GS} = 0
$r_{DS(on)}$	Static Drain-Source "ON" Resistance	–	150	Ohms	I_D = 0.1 mAdc, V_{GS} = 0

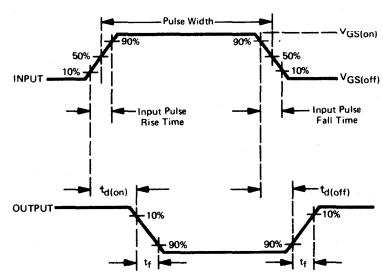
SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	–	5.0	ns	V_{DD} = 10 Vdc, $I_{D(on)}$ = 7.0 mAdc, $V_{GS(on)}$ = 0, $V_{GS(off)}$ = -10 Vdc
t_r	Rise Time	–	5.0	ns	
$t_{d(off)}$	Turn-Off Delay Time	–	15	ns	
t_f	Full Time	–	10	ns	

SWITCHING TIMES TEST CIRCUIT



INPUT PULSE
Rise Time < 1.0 ns
Fall Time < 1.0 ns
Nominal Value of "on" Pulse Width = 400 ns
Duty Cycle ≤ 1.0%
Generator Source Impedance = 50 Ohms



Intersil

N–CHANNEL SILICON EPITAXIAL J FET

2N5638 2N5639 2N5640

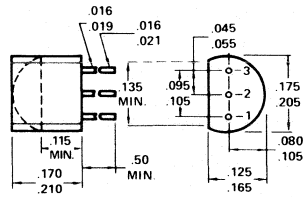
FEATURES

For analog switches, commutator and choppers.

- Economy Packaging
- Fast Switching – $t_{rise} < 5$ nsec (2N5638)
- Low Drain-Source 'ON' Resistance $< 30\ \Omega$ (2N5638)

PACKAGE DIMENSIONS

TO-92



PIN	OUT
1	D
2	S
3	G

5001B

ABSOLUTE MAXIMUM RATINGS

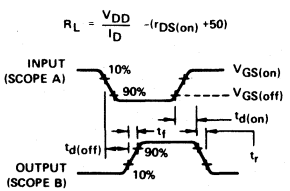
Drain-Source Breakdown Voltage	30 V
Drain-Gate Breakdown Voltage	30 V
Source-Gate Breakdown Voltage	30 V
Forward Gate Current	10 mA
Total Device Dissipation at 25°C	310 mW
Derate above 25°C	2.82 mW/°C
Operating Junction Temperature Range	-65 to +135°C
Storage Temperature Range	-65 to +150°C

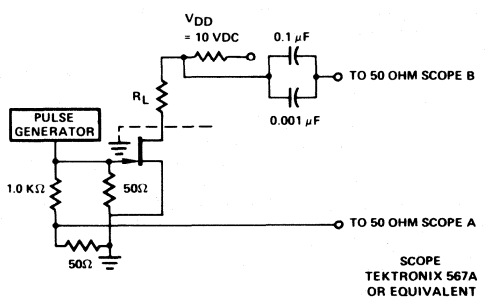
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

CHARACTERISTIC*		2N5638		2N5639		2N5640		UNIT	TEST CONDITIONS	
		MIN	MAX	MIN	MAX	MIN	MAX			
BV_{GSS}	Gate Reverse Breakdown Voltage	-30		-30		-30		V	$I_G = -10\ \mu A$, $V_{DS} = 0$	
I_{GSS}	Gate Reverse Current		-1.0		-1.0		-1.0	nA	$V_{GS} = -15$ V, $V_{DS} = 0$	
			-1.0		-1.0		-1.0	μA		$T_A = +100°C$
$I_{D(off)}$	Drain Cutoff Current		1.0		1.0		1.0	nA	$V_{DS} = 15$ V, $V_{GS} = -12$ V (2N5638)	
			1.0		1.0		1.0	μA	$V_{GS} = -8$ V (2N5639), $V_{GS} = -6$ V (2N5640)	$T_A = +100°C$
I_{DSS}	Saturation Drain Current	50		25		5.0		mA	$V_{DS} = 20$ V, $V_{GS} = 0$ (Note 1)	
$V_{DS(on)}$	Drain-Source ON Voltage		0.5		0.5		0.5	V	$V_{GS} = 0$, $I_D = 12$ mA (2N5638), $I_D = 6$ mA (2N5639), $I_D = 3$ mA (2N5640)	
$r_{DS(on)}$	Static Drain-Source ON Resistance		30		60		100	Ω	$I_D = 1$ mA, $V_{GS} = 0$	
$r_{ds(on)}$	Drain-Source ON Resistance		30		60		100		$V_{GS} = 0$, $I_D = 0$	f = 1 kHz
C_{iss}	Common-Source Input Capacitance		10		10		10	pF	$V_{GS} = -12$ V, $V_{DS} = 0$	f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		4.0		4.0		4.0			
$t_{d(on)}$	Turn-On Delay Time		4.0		6.0		8.0	ns	$V_{DD} = 10$ V, $I_{D(on)} = 12$ mA (2N5638)	
t_r	Rise Time		5.0		8.0		10		$V_{GS(on)} = 0$, $I_{D(on)} = 6$ mA (2N5639)	
t_d	Turn-OFF Delay Time		5.0		10		15		$V_{GS(off)} = -10$ V, $I_{D(on)} = 3$ mA (2N5640)	
t_f	Fall Time		10		20		30		$R_G = 50\ \Omega$	

*JEDEC registered data

NOTE:
1. Pulse test PW ≤ 300 μs, duty cycle ≤ 3.0%.





GENERAL DESCRIPTION

Matched FET pairs for differential amplifiers.

FEATURES

- Tracking $< 5\ \mu V/^{\circ}C$
- $I_G < 1$ pa
- Matched V_{GS}, $\Delta V_{GS}/\Delta T$, g_{fs}, & g_{oss}

Intersil

DUAL MONOLITHIC MATCHED N-CHANNEL JFETs (PAIR)

2N5902 thru 2N5909

ABSOLUTE MAXIMUM RATINGS

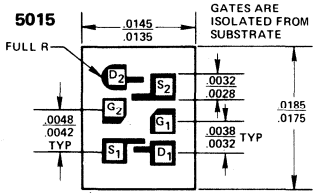
@ 25°C (unless otherwise noted)

Gate-Drain or Gate-Source Voltage	-40 V
Gate Current	10 mA
Device Dissipation (Each Side), $T_A = 25^{\circ}C$ (Derate 3 mW/°C)	367 mW
Total Device Dissipation, $T_A = 25^{\circ}C$ (Derate 4 mW/°C)	500 mW
Storage Temperature Range	-65°C to +150°C

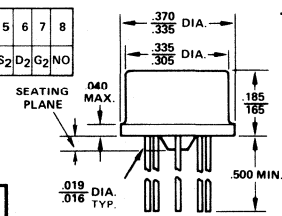
ORDERING INFORMATION

TO99	WAFER	CHIP
2N5902	2N5902/W	2N5902/D
2N5903	2N5903/W	2N5903/D
2N5904	2N5904/W	2N5904/D
2N5905	2N5905/W	2N5905/D
2N5906	2N5906/W	2N5906/D
2N5907	2N5907/W	2N5907/D
2N5908	2N5908/W	2N5908/D
2N5909	2N5909/W	2N5909/D

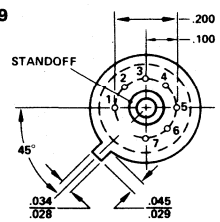
PACKAGE DIMENSIONS



PIN	1	2	3	4	5	6	7	8
OUT	S_1	D_1	G_1	CASE	S_2	D_2	G_2	NO



TO-99



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N5902-5 MIN	2N5902-5 MAX	2N5906-9 MIN	2N5906-9 MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		-5		-2	pA	$V_{GS} = -20$ V, $V_{DS} = 0$	
			-10		-5	nA		125°C
BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.6	-4.5	-0.6	-4.5		$V_{DS} = 10$ V, $I_D = 1$ nA	
V_{GS}	Gate Source Voltage		-4		-4			
I_G	Gate Operating Current		-3		-1	pA	$V_{DG} = 10$ V, $I_D = 30\ \mu A$	
			-3		-1	nA		125°C
I_{DSS}	Saturation Drain Current	30	500	30	500	μA		
g_{fs}	Common-Source Forward Transconductance	70	250	70	250	μmho	$V_{DS} = 10$ V, $V_{GS} = 0$	f = 1 kHz
g_{os}	Common-Source Output Conductance		5		5			
C_{iss}	Common-Source Input Capacitance		3		3	pF		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		1.5		1.5			
g_{fs}	Common-Source Forward Transconductance	50	150	50	150	μmho	$V_{DG} = 10$ V, $I_D = 30\ \mu A$	f = 1 kHz
g_{os}	Common-Source Output Conductance		1		1			
$\overline{e_n}$	Equivalent Short Circuit Input Noise Voltage		0.2		0.1	$\frac{\mu V}{\sqrt{Hz}}$	$V_{DS} = 10$ V, $V_{GS} = 0$	f = 100 Hz
NF	Spot Noise Figure		3		1	dB		$R_G = 10$ M

PARAMETER		2N5902-6 MIN	2N5902-6 MAX	2N5903-7 MIN	2N5903-7 MAX	2N5904-8 MIN	2N5904-8 MAX	2N5905-9 MIN	2N5905-9 MAX	UNIT	TEST CONDITIONS	
$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		2.0		2.0		2.0		2.0	nA	$V_{DG} = 10$ V, $I_D = 30\ \mu A$, $T_A = 125^{\circ}C$	2N5902-5
			0.2		0.2		0.2		0.2			2N5906-9
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio	0.95	1	0.95	1	0.95	1	0.95	1	—	$V_{DS} = 10$ V, $V_{GS} = 0$	
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio	0.97	1	0.97	1	0.95	1	0.95	1		$V_{DG} = 10$ V, $I_D = 30\ \mu A$	f = 1 kHz
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		5		10		15	mV		
$\frac{\Delta\lvert V_{BS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Measured at end points T_A and T_B)		5		10		20		40	$\mu V/^{\circ}C$		$T_A = 25^{\circ}C$, $T_B = 125^{\circ}C$
			5		10		20		40			$T_A = -55^{\circ}C$, $T_B = 25^{\circ}C$
$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		0.2		0.2		0.2		0.2	μmho		f = 1 kHz

FEATURES

- Tracking $< 20\ \mu V/^{\circ}C$
- $g_{fs} < 5000\ \mu mho$, 0 –100 MHz
- Matched V_{GS}, $\Delta V_{GS}/\Delta T$, I_G, g_{fs},

DUAL MONOLITHIC MATCHED N-CHANNEL JFETS (PAIR)

2N5911 2N5912

GENERAL DESCRIPTION

Matched FET pairs for wideband differential amplifiers.

ABSOLUTE MAXIMUM RATINGS

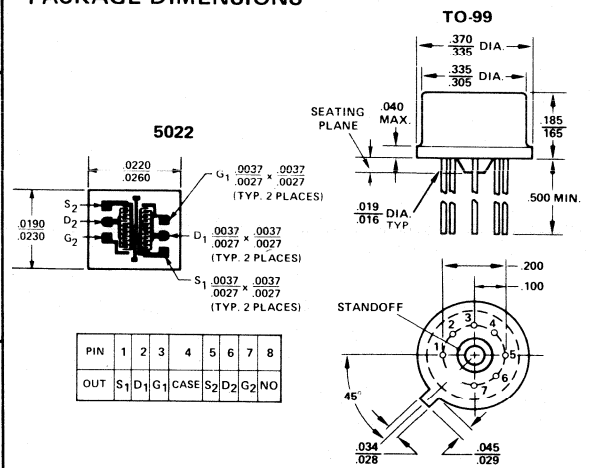
@ 25°C (unless otherwise noted)

Gate-Drain or Gate-Source Voltage	-25V
Gate Current	50 mA
Device Dissipation (Each Side),	367 mW
Linear Derating	3 mW/°C
Total Device Dissipation,	500 mW
Linear Derating	4 mW/°C
Storage Temperature Range	-65°C to +200°C

ORDERING INFORMATION

TO99	WAFER	CHIP
2N5911	2N5911/W	2N5911/D
2N5912	2N5912/W	2N5911/D

PACKAGE DIMENSIONS



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		MIN	MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		-100	pA	V_{GS} = -15 V, V_{DS} = 0	
			-250	nA		150°C
BV_{GSS}	Gate Reverse Breakdown Voltage	-25		V	I_G = -1 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-5		V_{DS} = 10 V, I_D = 1 nA	
V_{GS}	Gate-Source Voltage	-0.3	-4		V_{DG} = 10 V, I_D = 5 mA	
I_G	Gate Operating Current		-100	pA		
			-100	nA		125°C
I_{DSS}	Saturation Drain Current (Pulsewidth 300 μs, duty cycle ≤ 3%)	7	40	mA	V_{DS} = 10 V, V_{GS} = 0 V	
g_{fs}	Common-Source Forward Transconductance	5000	10,000	μmho	V_{DG} = 10 V, I_D = 5 mA	f = 1 kHz
g_{fs}	Common-Source Forward Transconductance	5000	10,000			f = 100 MHz
g_{os}	Common-Source Output Conductance		100			f = 1 kHz
g_{oss}	Common-Source Output Conductance		150			f = 100 MHz
C_{iss}	Common-Source Input Capacitance		5	pF		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			
$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		20	$\frac{nV}{\sqrt{Hz}}$		f = 10 kHz
NF	Spot Noise Figure		1	dB		f = 10 kHz, R_G = 100KΩ

PARAMETER		2N5911 MIN	2N5911 MAX	2N5912 MIN	2N5912 MAX	UNIT	TEST CONDITIONS	
$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		20		20	nA	V_{DG} = 10 V, I_D = 5 mA	125°C
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio	0.95	1	0.95	1		V_{DS} = 10 V, V_{GS} = 0 (Pulsewidth 300 μs, duty cycle ≤ 3%)	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		10		15	mV	V_{DG} = 10 V, I_D = 5 mA	
$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Measured at end points, T_A and T_B)		20		40	μV/°C		T_A = 25°C, T_B = 125°C
			20		40			T_A = -55°C, T_B = 25°C
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio	0.95	1	0.95	1			f = 1 kHz

Intersil

LOW NOISE DUAL MONOLITHIC MATCHED N-CHANNEL JFETS

2N6483 2N6484 2N6485

FEATURES

- Ultra Low Noise
  $\bar{e}_n < 10\ nV/\sqrt{Hz}$ at 10 Hz
- High CMRR > 100 dB
- Low Offset
  $\Delta\ |\ V_{GS1} - V_{GS2}\ | < 5\ mV$
- Tight Tracking
  $\Delta\ |\ V_{GS1} - V_{GS2}\ | / \Delta T < 5\ \mu V/°C$

GENERAL DESCRIPTION

These N-Channel Junction FETs are characterized for ultra low noise applications requiring tightly controlled and specified noise parameters at 10 Hz and 1000 Hz. Tight matching specifications make these devices ideal as the input stage for low frequency differential, instrumentation amplifiers.

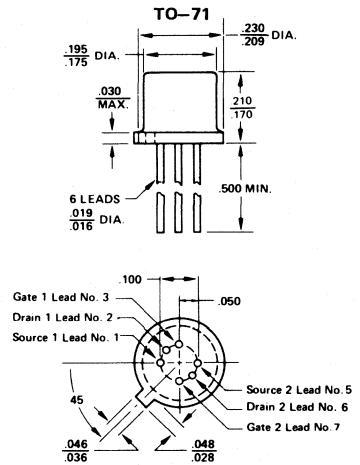
ABSOLUTE MAXIMUM RATINGS (Note 1)

(@ 25°C unless otherwise noted)

Maximum Temperatures	
Storage Temperature	-65°C to +150°C
Operating Junction Temperature	+150°C
Lead Temperature (soldering, 10 sec. time limit)	+300°C
Maximum Power Dissipation	
Device Dissipation @ 85°C Free Air Temperature	
One Side	250 mW
Both Sides	500 mW
Linear Derating	
One Side	3.85 mW/°C
Both Sides	7.7 mW/°C
Maximum Voltages & Currents	
V_{GS} Gate to Source Voltage	-50 V
V_{GD} Gate to Drain Voltage	-50 V
$V_{G1\ G2}$ Gate to Gate Voltage	±50 V
I_G Gate Current	50 mA

PACKAGE DIMENSIONS

TO-71



5019

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise specified)

SYMBOL	CHARACTERISTICS	MIN.	MAX.	UNIT	TEST CONDITIONS
I_{GSS}	Gate Reverse Current		200 200	pA nA	V_{GS} = -30 V, V_{DS} = 0, T_A = +25°C V_{GS} = -30 V, V_{DS} = 0, T_A = +150°C
BV_{GSS}	Gate-Source Breakdown Voltage	50		V	I_G = -1 μA, V_{DS} = 0
V_p	Gate-Source Pinch-Off Voltage	0.7	-4.0	V	V_{DS} = 20 V, I_D = 1 nA
I_{DSS}	Drain Current at Zero Gate Voltage	0.5	7.5	mA	V_{DS} = 20 V, V_{GS} = 0 (Note 2)
g_{fs}	Common-Source Forward Transconductance	1000	4000	μmho	V_{DS} = 20 V, V_{GS} = 0, f = 1 KHz (Note 2)
g_{oss}	Common-Source Output Conductance		10	μmho	V_{DS} = 20 V, V_{GS} = 0, f = 1 KHz
C_{iss}	Common-Source Input Capacitance		20	pF	V_{DS} = 20 V, V_{GS} = 0, f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		3.5	pF	V_{DS} = 20 V, V_{GS} = 0, f = 1 MHz
I_G	Gate Current		-100 -100	pA nA	V_{GD} = 20 V, I_D = 200 μA, T_A = +25°C V_{DG} = 20 V, I_D = 200 μA, T_A = +150°C
V_{GS}	Gate-Source Voltage	-0.2	-3.8	V	V_{DG} = 20 V, I_D = 200 μA
g_{fs}	Common-Source Forward Transconductance	500	1500	μmho	V_{DG} = 20 V, I_D = 200 μA, f = 1 KHz (Note 2)
g_{os}	Common-Source Output Conductance		1	μmho	V_{DG} = 20 V, I_D = 200 μA
$\bar{e}_n$	Equivalent Input Noise Voltage		10 5	$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$	V_{DS} = 20 V, I_D = 200 μA, f = 10 Hz V_{DS} = 20 V, I_D = 200 μA, f = 1 KHz

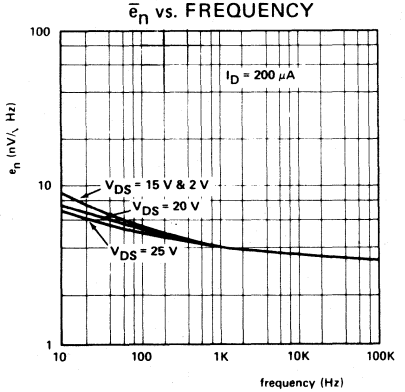
MATCHING CHARACTERISTICS (@ 25°C unless otherwise noted)

SYMBOL	CHARACTERISTIC	2N6483		2N6484		2N6485		UNIT	CONDITIONS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\frac{I_{DSS1}}{I_{DSS2}}$	Drain Current Ratio at Zero Gate Voltage	0.95	1	0.95	1	0.95	1	–	V_{DS} = 20 V, V_{GS} = 0 (Note 2)
$\lvert I_{G1} - I_{G2} \rvert$	Differential Gate Current		10		10		10	nA	V_{DG} = 20 V, I_D = 200 μA T_A = +125°C
$\frac{g_{fs1}}{g_{gs2}}$	Transconductance Ratio	0.97	1	0.97	1	0.95	1	–	V_{DG} = 20 V, I_D = 200 μA, f = 1 KHz (Note 2)
$\lvert g_{os1} - g_{os2} \rvert$	Differential Output Conductance		0.1		0.1		0.1	μmho	V_{DG} = 20 V, I_D = 200 μA, f = 1 KHz
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage		5		10		15	mV	V_{DG} = 20 V, I_D = 200 μA
$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift		5		10		25	μV/°C	V_{DG} = 20 V, I_D = 200 μA T_A = +25°C to +125°C
$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift		5		10		25	μV/°C	V_{DG} = 20 V, I_D = 200 μA T_A = -55°C to + 25°C
CMRR	Common Mode Rejection Ratio	100		100		90		dB	V_{DD} = 10 to 20 V, I_D = 200 μA (Note 3)

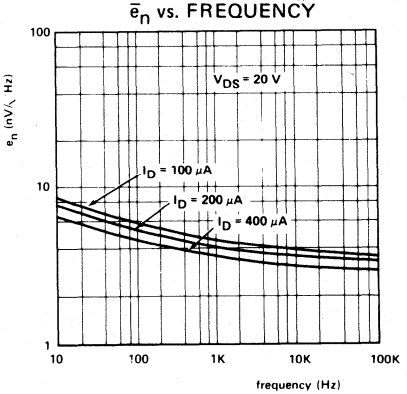
NOTES: 1. These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
2. Pulse duration of 2 ms used during test.
3. CMRR = $20\text{Log}_{10}\Delta V_{DD}/\Delta\lvert V_{GS1} - V_{GS2}\rvert$, ($\Delta V_{DD}$ = 10 V), not included in JEDEC registration

TYPICAL CHARACTERISTICS OF 2N6483, 2N6484, 2N6485

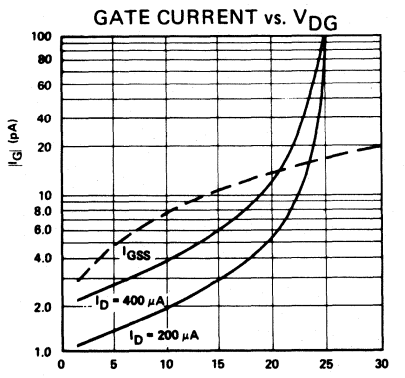
$\bar{e}_n$ vs. FREQUENCY



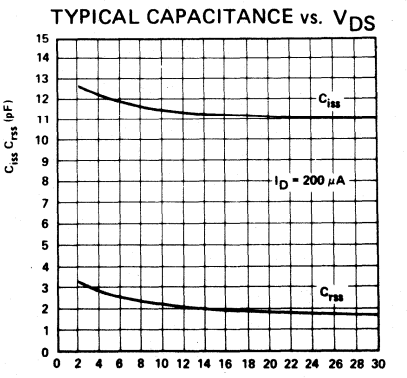
$\bar{e}_n$ vs. FREQUENCY



GATE CURRENT vs. V_{DG}



TYPICAL CAPACITANCE vs. V_{DS}



GENERAL DESCRIPTION

These devices are a dual P-channel, silicon, tetrode, insulated gate, enhancement-type, field-effect transistors designed primarily for low power chopper and switching applications. These devices include a shunting resistor diode network connected between the gate and body.

Intersil

DUAL MATCHED P-CHANNEL ENHANCEMENT MODE MOS FETS (DIODE PROTECTED)

3N147 3N148

ABSOLUTE MAXIMUM RATINGS (Note 2)

Maximum Temperatures

Operating Junction Temperature	−65°C to +175°C
Storage Temperature	−65°C to +200°C
Lead Temperature (Soldering, 10 sec time limit)	+300°C

Maximum Power Dissipation (Note 3)

Total Dissipation at 25°C Case Temperature	1.7W
at 25°C Ambient Temperature	0.6 W

Maximum Voltages and Currents

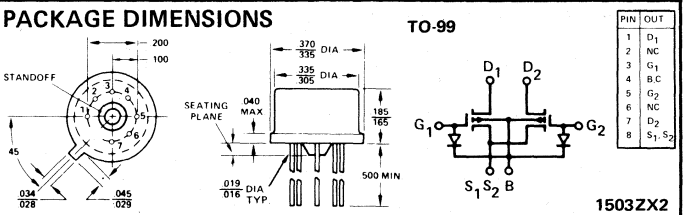
$V_{GS(f)}$	Forward Gate to Bulk Voltage	−50 V
V_{DB}	Drain to Bulk Voltage	−30 V
V_{SB}	Source to Bulk Voltage	−30 V
I_G	Gate Current	10 mA
I_D	Drain Current	200 mA
I_S	Source Current	200 mA
I_B	Bulk Current	200 mA

FEATURES

- Integrated Gate Protection Circuit (Note 1)
- Low On-Resistance $r_{ds(on)}$ = 500 Ω (Max)
- Low Leakage $I_{D(off)}$ = 0.5 nA (Max)

PACKAGE DIMENSIONS

TO-99



1503ZX2

ELECTRICAL CHARACTERISTICS (Each Side, 25°C Free Air Temperature unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNITS	TEST CONDITIONS	
$V_{GB(f)}$	Forward Gate Voltage (Note 4)		−50			V	I_G = 10 mA	$V_{DB} = V_{SB} = 0$
$V_{(BR)DB}$	Drain to Bulk Breakdown Voltage		−30			V	I_D = 10 μA	$V_{GB} = V_{SB} = 0$
$V_{(BR)SB}$	Source to Bulk Breakdown Voltage		−30			V	I_S = 10 μA	$V_{GB} = V_{DB} = 0$
$I_{D(off)}$	Drain Off Current	3N147		1.0	5.0	nA	V_{DB} = −20 V	$V_{GB} = V_{SB} = 0$
		3N148		0.1	0.5	nA	V_{DB} = −20 V	$V_{GB} = V_{SB} = 0$
$I_{S(off)}$	Source Off Current	3N147		2.0	10	nA	V_{SB} = −20 V	$V_{GB} = V_{DB} = 0$
		3N148		0.2	1.0	nA	V_{SB} = −20 V	$V_{GB} = V_{DB} = 0$
$I_{G(f)}$	Gate Forward Current			0.03	1.0	nA	V_{GB} = −40 V	$V_{DB} = V_{SB} = 0$
$V_{GS(th)}$	Gate to Source Threshold Voltage		−2.0	−3.6	−6.0	V	I_D = 10 μA	V_{DS} = −20 V $V_{BS} = 0$
$V_{GS(th)}$	Gate to Source Threshold Voltage		−3.0	−6.8	−12	V	I_D = 10 μA	V_{DS} = −20 V V_{BS} = 5.0 V
$V_{GS(th)}$	Gate to Source Threshold Voltage		−4.0	−8.0	−15	V	I_D = 10 μA	V_{DS} = −20 V V_{BS} = 10 V
$I_{D(on)}$	On-state Drain Current		8.0	22		mA	V_{DS} = −20 V	V_{GS} = −15 V $V_{BS} = 0$
$V_{DS(on)}$	Drain to Source On-state Voltage			−1.2	−2.5	V	I_D = 5.0 mA	V_{GS} = −15 V $V_{BS} = 0$
$r_{ds(on)}$	Drain to Source On-state Resistance (f = 1.0 kHz)			205	500	Ω	V_G = −15 V	$V_D = 0$ $V_S = 0$ $V_B = 0$
$r_{ds(on)}$	Drain to Source On-state Resistance (f = 1.0 kHz)			220	650	Ω	V_G = −25 V	V_D = −5.0 V V_S = −5.0 V V_B = 5.0 V
$r_{ds(on)}$	Drain to Source On-state Resistance (f = 1.0 kHz)			270	800	Ω	V_G = −30 V	V_D = −10 V V_S = −10 V V_B = 10 V

ELECTRICAL CHARACTERISTICS (Each Side, 25°C Free Air Temperature unless otherwise noted)

PARAMETER			MIN	MAX	UNITS	TEST CONDITIONS	
C_d	Drain Capacitance (f = 1.0 MHz)		8.0	12	pF	$V_{DB} = 0$	$V_{SB} = V_{GB} = 0$
C_s	Source Capacitance (f = 1.0 MHz)		14	20	pF	$V_{SB} = 0$	$V_{DB} = V_{GB} = 0$
C_g	Gate Capacitance (f = 1.0 MHz)		4.2	6.0	pF	V_{GB} = −40 V	$V_{DB} = V_{SB} = 0$
C_{dg}	Drain to Gate Capacitance (f = 1.0 MHz)		0.8	2.0	pF	$V_{DG} = 0$	$V_{BS} = 0$
C_{sg}	Source to Gate Capacitance (f = 1.0 MHz)		0.8	2.0	pF	$V_{SG} = 0$	$V_{BS} = 0$
$t_{d(on)}$	Turn On Delay Time		4.0	20	ns	V_{DD} = −17.5 V	$I_{D(on)}$ = 5.0 mA
t_r	Rise Time		30	100	ns	$V_{GS(on)}$ = −15 V	$V_{GS(off)} = 0$
$t_{d(off)}$	Turn Off Delay Time		6.0	30	ns	R_G = 50 Ω	
t_r	Fall Time		100	150	ns		
$I_{D(off)}(125°C)$	Drain Off Current	3N147	1.0	5.0	μA	V_{DB} = −20 V	$V_{GB} = V_{SB} = 0$
		3N148	0.1	0.5	μA	V_{DB} = −20 V	$V_{GB} = V_{SB} = 0$
$I_{S(off)}(125°C)$	Source Off Current	3N147	2.0	10	μA	V_{SB} = −20 V	$V_{GB} = V_{DB} = 0$
		3N148	0.2	1.0	μA	V_{SB} = −20 V	$V_{GB} = V_{DB} = 0$
$I_{G(f)}(125°C)$	Gate Forward Leakage Current		0.03	1.0	μA	V_{GB} = −40 V	$V_{DB} = V_{SB} = 0$
$r_{ds(on)}(125°C)$	Drain to Source On Resistance (f = 1.0 kHz)		345	850	Ω	V_G = −15 V	$V_D = 0$ $V_S = 0$ $V_B = 0$
$r_{ds(on)}(125°C)$	Drain to Source On Resistance (f = 1.0 kHz)		0.36	1.1	kΩ	V_G = −25 V	V_D = −5.0 V V_S = −5.0 V V_B = 5.0 V
$r_{ds(on)}(125°C)$	Drain to Source On Resistance (f = 1.0 kHz)		0.32	1.35	kΩ	V_G = −30 V	V_D = −10 V V_S = −10 V V_B = 10 V

NOTES:

1. The Integrated Gate Protection Circuit consists of a diffused resistor-diode network which protects the gate of the MOS-FET from accidental damage due to voltage transients.
2. These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
3. These ratings give a maximum junction temperature of 175°C and junction to case thermal resistance of 88.2°C/Watt (derating factor of 11.3 mW/°C); junction to ambient thermal resistance of 250°C/Watt (derating factor of 4.0 mW/°C).
4. Pulse Condition: Pulse width ≤ 1.0 ms; Duty Cycle = 1%.

Intersil

P-CHANNEL ENHANCEMENT MODE MOS FET

3N160

GENERAL DESCRIPTION

ENHANCEMENT-TYPE METAL-OXIDE SEMICONDUCTOR TRANSISITOR

For applications requiring very high input impedance, such as series and shunt choppers, multiplexers, and commutators.

- Channel Cut Off with Zero Gate Voltage
- Square-Law Transfer Characteristic Reduces Distortion
- Independent Substrate Connection Provides Flexibility in Biasing

ABSOLUTE MAXIMUM RATINGS

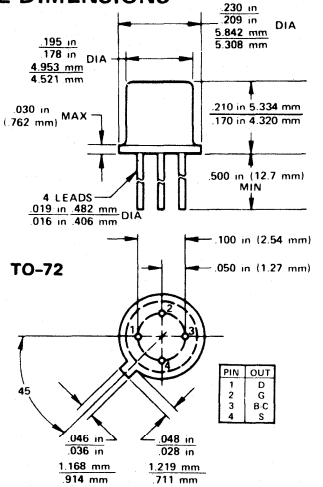
@25°C free-air temperature (unless otherwise noted)

Drain-Gate Voltage	-25 V
Drain-Source Voltage	-25 V
Forward Gate-Source Voltage	-25 V
Reverse Gate-Source Voltage	+25 V
Continuous Drain Current	-125 mA
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature	360 mW
Continuous Device Dissipation at (or below) 25°C Case Temperature	1.8 W
Storage Temperature Range	-65°C to 200°C
Lead Temperature 1/16 Inch from Case for 10 Seconds	300°C

HANDLING PRECAUTIONS

Curve-tracer testing and static-charge buildup are common causes of damage to insulated-gate devices. Permanent damage may result if either gate-voltage rating is exceeded even for extremely short time periods. Each transistor is protected during shipment by a gate-shorting device, which should be removed only during testing and after permanent mounting of the transistor. Personnel and equipment, including soldering irons, should be grounded.

PACKAGE DIMENSIONS



1503X2

ELECTRICAL CHARACTERISTICS (25°C free-air temperature unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT	TEST CONDITIONS	
I_{GSSF}	Forward Gate-Terminal Current		<-1	-50	pA	V_{GS} = -25 V, V_{DS} = 0	
			-10	-50	pA	V_{GS} = -25 V, V_{DS} = 0,	T_A = 100°C
I_{GSSR}	Reverse Gate-Terminal Current		<1	10	pA	V_{GS} = 25 V, V_{DS} = 0	
I_{DSS}	Zero-Gate-Voltage Drain Current		<1	-10	nA	V_{DS} = -15 V, V_{GS} = 0	
				-10	μA	V_{DS} = -25 V, V_{GS} = 0	
$V_{GS(th)}$	Gate-Source Threshold Voltage	-1.5		-5	V	V_{DS} = -15 V, I_D = -10 μA	
V_{GS}	Gate-Source Voltage	-4.5		-8	V	V_{DS} = -15 V, I_D = -8 mA	
$I_{D(on)}$	On-State Drain Current	-40		-120	mA	V_{DS} = -15 V, V_{GS} = -15 V,	
$\|y_{fs}\|$	Small-Signal Common-Source Forward Transfer Admittance	3.5		6.5	mmho	V_{DS} = -15 V I_D = -8 mA	f = 1 kHz
$\|y_{os}\|$	Small-Signal Common-Source Output Admittance			0.25	mmho		
C_{iss}	Common-Source Short-Circuit Input Capacitance			10	pF		f = 1 MHz
C_{rss}	Common-Source Short-Circuit Reverse Transfer Capacitance			4	pF		

DIODE PROTECTED P-CHANNEL ENHANCEMENT MODE MOS FET

3N161

GENERAL DESCRIPTION

DIODE-PROTECTED ENHANCEMENT-TYPE METAL-OXIDE-SEMICONDUCTOR TRANSISTOR

For applications requiring very high input impedance, such as series and shunt choppers, multiplexers, and commutators.

FEATURES

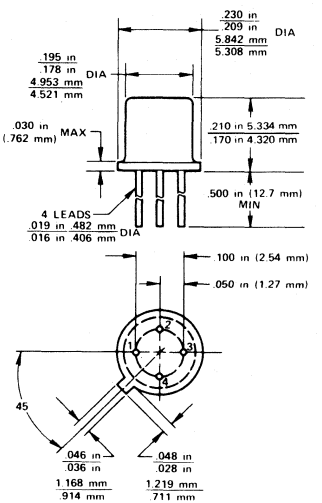
- Channel Cut Off with Zero Gate Voltage
- Square-Law Transfer Characteristic Reduces Distortion
- Independent Substrate Connection Provides Flexibility in Biasing
- Internally Connected Diode Protects Gate from Damage due to Overvoltage

DESCRIPTION

These devices are designed for applications requiring very high input impedance, such as choppers, commutators, and logic switches. Each device is protected from excessive input voltage by a shunting diode connected from the gate to the source. This eliminates the need for most precautionary handling procedures associated with unprotected MOS devices.

PACKAGE DIMENSIONS

TO-72



PIN	OUT
1	D
2	G
3	B C
4	S

1503ZX2

ELECTRICAL CHARACTERISTICS (25°C free-air temperature unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT	TEST CONDITIONS	
I_{GSSF}	Forward Gate-Terminal Current			−0.1	nA	V_{GS} = −25 V, V_{DS} = 0	
				−1	nA	V_{GS} = −25 V, V_{DS} = 0,	T_A = 100°C
$V_{(BR)GSSF}$	Forward Gate-Source Breakdown Voltage	−25			V	I_G −0.1 mA, V_{DS} = 0,	
I_{DSS}	Zero-Gate-Voltage Drain Current			−10	nA	V_{DS} = −15 V, V_{GS} = 0	
				−10	μA	V_{DS} = −25 V, V_{GS} = 0	
$V_{GS(th)}$	Gate-Source Threshold Voltage	−1.5		−5	V	V_{DS} = −15 V, I_D = 10 μA	
V_{GS}	Gate-Source Voltage	−4.5		−8	V	V_{DS} = −15 V, I_D = −8 mA	
$I_{D(on)}$	On-State Drain Current	−40		−120	mA	V_{DS} = −15 V, V_{GS} = −15 V, See Note 4	
$\lvert y_{fs} \rvert$	Small-Signal Common-Source Forward Transfer Admittance	3500		6500	μmho	V_{DS} = −15 V, I_D = −8 mA	f = 1 kHz
$\lvert y_{os} \rvert$	Small-Signal Common-Source Output Admittance			250	μmho		
C_{iss}	Common-Source Short-Circuit Input Capacitance			10	pF		f = 1 MHz
C_{rss}	Common-Source Short-Circuit Reverse Transfer Capacitance			4	pF		

FEATURES

- Very High Input Impedance
- High Gate Breakdown
- Fast Switching
- Low Capacitance

Intersil

P-CHANNEL ENHANCEMENT MODE MOS FET

3N163

MAXIMUM RATINGS

(@ 25°C ambient unless noted)

		3N163
V_{GSS}	Static Gate to Source Voltage	±40 V
V_{GSS}(1)	Transient Gate to Source Voltage	±125V
V_{DSS}	Drain to Source Voltage	-40 V
V_{SDS}	Source to Drain Voltage	-40 V
V_{DGO}	Drain to Gate Voltage	-40 V
I_D	Drain Current	-50 mA
P_D	Power Dissipation	375 mW
	Derating Factor	3.0 mW/°C
T_j	Operating Junction Temperature	-55 to +150°C
T_{sto}	Storage Temperature	-65 to +200°C
T_l	Lead Temperature 1/16" from Case for 10 sec max	+265°C

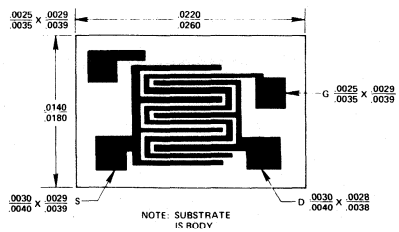
(1) Devices must not be tested at ±125V more than once or for longer than 300 ms.

ORDERING INFORMATION

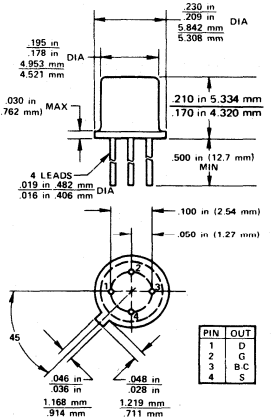
TO72	WAFER	CHIP
3N163	3N163/W	3N163/D

PACKAGE DIMENSIONS

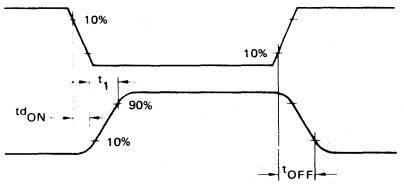
1503



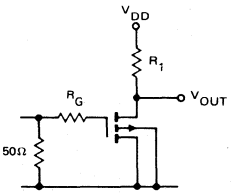
TO-72



SWITCHING WAVEFORM



SWITCHING TIME CIRCUIT



ELECTRICAL CHARACTERISTICS (@ 25°C and V_{BS} = 0 unless noted)

PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS
I_{GSS}	Gate Reverse Leakage Current		10	pA	V_{GS} = 40 V
$I_{G(f)}$	Gate Forward Current		-10	pA	V_{GS} = -40 V
$I_{G(f)}$	Gate Forward Current @ 125°C		-25	pA	V_{GS} = -40 V
BV_{DSS}	Drain-Source Breakdown Voltage	-40		V	I_D = -10 μA, V_{GS} = 0
BV_{SDS}	Source Drain Breakdown Voltage	-40		V	I_S = -10 μA, V_{GD} = 0, V_{DB} = 0
$V_{GS(th)}$	Threshold Voltage	-2.0	-5.0	V	V_{DS} = V_{GS}, I_D = -10 μA
$V_{GS(th)}$	Threshold Voltage	-2.0	-5.0	V	V_{DS} = -15 V, I_D = -10 μA
V_{GS}	Gate Source Voltage	-3.0	-6.5	V	V_{DS} = -15 V, I_D = 0.5 mA
I_{DSS}	Zero Gate Voltage Drain Current		-200	pA	V_{DS} = -15 V, V_{GS} = 0
I_{SDS}	Source Drain Current		-400	pA	V_{SD} = 15 V, V_{GS} = V_{DB} = 0
$r_{ds(on)}$	Drain-Source on Resistance		250	ohms	V_{GS} = -20 V, I_D = -100 μA
$I_{D(on)}$	On Drain Current	-5.0	-30.0	mA	V_{DS} = -15 V, V_{GS} = -10 V
g_{fs}	Forward Transconductance @ 1 kHz	2000	4000	μmhos	V_{DS} = -15 V, I_D = -10 mA, f = 1kHz
g_{oss}	Output Admittance @ 1 kHz		250	μmhos	V_{DS} = -15 V, I_D = -10 mA, f = 1kHz
C_{iss}	Input Capacitance – Output Shorted		2.5	pF	V_{DS} = -15 V, I_D = -10 mA, f = 1MHz
C_{rss}	Reverse Transfer Capacitance		0.7	pF	V_{DS} = -15 V, I_D = -10 mA, f = 1MHz
C_{oss}	Output Capacitance Input Shorted		3.0	pF	V_{DS} = -15 V, I_D = -10 mA, f = 1 MHz

SWITCHING CHARACTERISTICS (@ 25°C and V_{BS} = 0)

t_{on}		12	ns	V_{DD} = -15 V
t_r		24	ns	$I_{D(on)}$ = 10 mA
t_{off}		50	ns	R_G = R_L = 1.5kΩ

FEATURES

- Very High Input Impedance
- High Gate Breakdown
- Low Capacitance

DUAL MATCHED P-CHANNEL ENHANCEMENT MODE MOS FETS

3N165 3N166

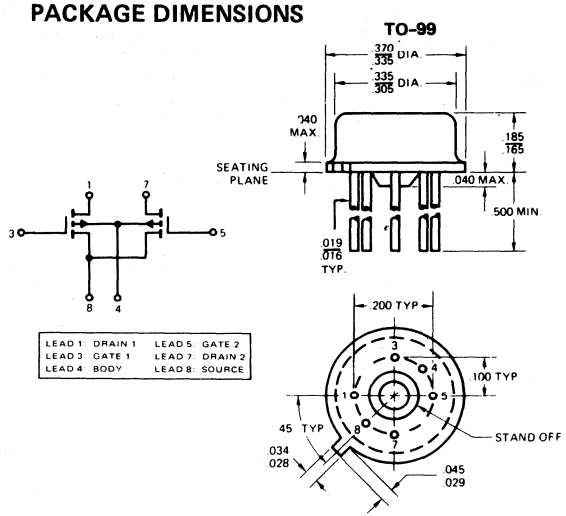
MAXIMUM RATINGS (@ 25°C ambient unless noted)

V_{GSS}	Static Gate to Source Voltage	±40V
V_{GSS} [1]	Transient Gate to Source Voltage	±125V
V_{DSS}	Drain to Source Voltage	-40V
V_{GDS}	Source to Drain Voltage	-40V
V_{OO}	Gate to Gate	±80V
V_G	Any Lead to Case	±40V
I_D	Drain Current	50 mA
P_D	Power Dissipation (each side)	300 mW
	(both sides)	525 mW
	Total Derating Factor	4.2 mW/°C
T_j	Operating Junction Temperature	-55 to +150°C
T_{stg}	Storage Temperature	-65 to +200°C
T_l	Lead Temperature 1/16" from Case for 10 sec max	+300°C

[1] Devices must not be tested at ±125V more than once or for longer than 300 ms.

PACKAGE DIMENSIONS

TO-99



ALL DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
BODY (SUBSTRATE) INTERNALLY CONNECTED TO METAL CASE
COMMON SOURCE AND SUBSTRATE CONNECTIONS

BOTTOM VIEW

2506

ELECTRICAL CHARACTERISTICS (@ 25°C and V_{BS} = 0 unless noted)

		3N165		3N166		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
I_{GSS}	Gate Reverse Leakage Current		10		10	pA	V_{GS} = 40V
$I_{G(f)}$	Gate Forward Leakage Current		-10		-10	pA	V_{GS} = -40V
$I_{G(f)}$	Gate Forward Leakage Current (+125°C)		-25		-25	pA	V_{GS} = -40V
I_{DSS}	Drain to Source Leakage Current		-200		-200	pA	V_{DS} = -20V
I_{SDS}	Source to Drain Leakage Current		-400		-400	pA	V_{SD} = -20V, V_{DB} = 0
$I_{D(on)}$	On Drain Current	-5	-30	-5	-30	mA	V_{DS} = -15V, V_{GS} = -10V
$V_{GS(th)}$	Gate Source Threshold Voltage	-2	-5	-2	-5	V	V_{DS} = -15V, I_D = -10 μA
$V_{GS(th)}$	Gate Source Threshold Voltage	-2	-5	-2	-5	V	V_{DS} = V_{GS}, I_D = -10 μA
$r_{ds(on)}$	Drain Source On Resistance		300		300	ohms	V_{GS} = -20V, I_D = -100 μA
g_{fs}	Forward Transconductance	1500	3000	1500	3000	μmhos	V_{DS} = -15V, I_D = -10 mA, f = 1 kHz
g_{os}	Output Admittance		300		300	μmhos	V_{DS} = -15V, I_D = -10 mA, f = 1 kHz
C_{iss}	Input Capacitance		3.0		3.0	pF	V_{DS} = -15V, I_D = -10 mA, f = 1 MHz
C_{rss}	Reverse Transfer Capacitance		0.7		0.7	pF	V_{DS} = -15V, I_D = -10 mA, f = 1 MHz
C_{oss}	Output Capacitance Input Shorted		3.0		3.0	pF	V_{DS} = -15V, I_D = -10 mA, f = 1 MHz
$R_E(Y_{fs})$	Real Part Forward Transconductance	1200			1200	μmhos	V_{DS} = -15V, I_D = -10 mA, f = 100 MHz

MATCHING CHARACTERISTICS 3N165

		MIN	MAX	UNITS	TEST CONDITIONS
Y_{fs1}/Y_{fs2}	Forward Transconductance Ratio	0.90	1.0		V_{DS} = -15V, I_D = -500 μA, f = 1 kHz
V_{GS1-2}	Gate-Source Threshold Voltage Differential		100	mV	V_{DS} = -15V, I_D = -500 μA
ΔV_{GS1-2}	Gate-Source Threshold Voltage Differential Change with Temperature		8	mV	V_{DS} = -15V, I_D = -500 μA T = -55°C to +25°C
ΔV_{GS1-2}	Gate-Source Threshold Voltage Differential Change with Temperature		10	mV	V_{DS} = -15V, I_D = -500 μA T = +25°C to +125°C

FEATURES

- Low Switching Voltages – $V_{GS(th)} \leq 3.0$ Vdc
- Fast Switching Times – $t_r \leq 10$ ns
- Low Drain-Source Resistance $r_{ds(on)} = 200$ Ohms (Max)
- Low Reverse Transfer Capacitance $C_{rss} = 1.3$ pF (Max)
- Manufactured Using the New Silicon Nitride Process Resulting in a Stable $V_{GS(th)}$ and Gate Oxide Breakdown Protection to Typical Transients of ±150 Volts Peak

Intersil

N-CHANNEL ENHANCEMENT MODE MOS FET

3N169
3N170
3N171

HANDLING PRECAUTIONS

MOS field-effect transistors have extremely high input resistance. They can be damaged by the accumulation of excess static charge. Avoid possible damage to the devices while wiring, testing, or in actual operation, by following the procedures outlined below:

1. To avoid the build-up of static charge, the leads of the devices should remain shorted together with a metal ring except when being tested or used.
2. Avoid unnecessary handling. Pick up devices by the case instead of the leads.
3. Do not insert or remove devices from circuits with the power on because transient voltages may cause permanant damage to the devices.

GENERAL DESCRIPTION

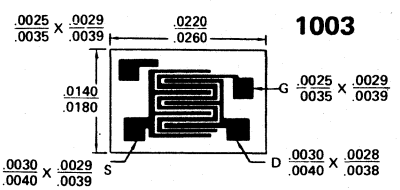
Enhancement Mode (Type C) transistors designed for low-power switching applications.

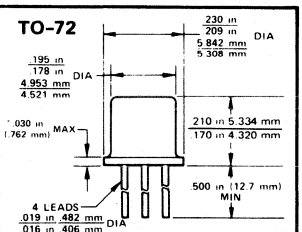
ORDERING INFORMATION

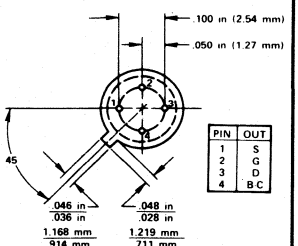
TO72	WAFER	CHIP
3N169	3N169/W	3N169/D
3N170	3N170/W	3N170/D
3N171	3N171/W	3N171/D

MAXIMUM RATINGS ($T_A = 25^\circ C$ unless otherwise noted)

RATING	SYMBOL	VALUE	UNIT
Drain-Source Voltage	V_{DS}	25	Vdc
Drain-Gate Voltage	V_{DG}	±35	Vdc
Gate-Source Voltage	V_{GS}	±35	Vdc
Drain Current	I_D	30	mAdc
Power Dissipation @ $T_A = 25^\circ C$	P_D	300	mW
Seperate above 25°C		1.7	mW/°C
Power Dissipation @ $T_C = 25^\circ C$	P_D	800	mW
Seperate above 25°C		4.56	mW/°C
Operating Junction Temperature	T_J	175	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C







ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ C$ unless otherwise noted) Substrate connected to source.

PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS
OFF CHARACTERISTICS					
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	25		Vdc	$I_D = 10\ \mu$Adc, $V_{GS} = 0$
I_{GSS}	*Gate Leakage Current		10	pAdc	$V_{GS} = -35$ Vdc, $V_{DS} = 0$
			100		$V_{GS} = -35$ Vdc, $V_{DS} = 0$, $T_A = 125^\circ C$
I_{DSS}	*Zero-Gate-Voltage Drain Current		10	nAdc	$V_{DS} = 10$ Vdc, $V_{GS} = 0$
			1.0	μAdc	$V_{DS} = 10$ Vdc, $V_{GS} = 0$, $T_A = 125^\circ C$
***ON CHARACTERISTICS**					
$V_{GS(th)}$	Gate-Source Threshold Voltage	0.5	1.5	Vdc	3N169
		1.0	2.0		$V_{DS} = 10$ Vdc, $I_D = 10\ \mu$Adc 3N170
		1.5	3.0		3N171
$I_{D(on)}$	"ON" Drain Current	10		mAdc	$V_{GS} = 10$ Vdc, $V_{DS} = 10$ Vdc
$V_{DS(on)}$	Drain-Source "ON" Voltage		2.0	Vdc	$I_D = 10$ mAdc, $V_{GS} = 10$ Vdc
SMALL SIGNAL CHARACTERISTICS					
$r_{ds(on)}$	*Drain-Source Resistance		200	Ohms	$V_{GS} = 10$ Vdc, $I_D = 0$, f = 1.0 kHz
$\lvert g_{fs} \rvert$	Forward Transfer Admittance	1000		μmhos	$V_{DS} = 10$ Vdc, $I_D = 2.0$ mAdc, f = 1.0 kHz
C_{rss}	*Reverse Transfer Capacitance		1.3	pF	$V_{DS} = 0$, $V_{GS} = 0$, f = 1.0 MHz
C_{iss}	*Input Capacitance		5.0	pF	$V_{DS} = 10$ Vdc, $V_{GS} = 0$, f = 1.0 MHz
$C_{d(sub)}$	*Drain-Substrate Capacitance		5.0	pF	$V_{D(SUB)} = 10$ Vdc, f = 1.0 MHz
***SWITCHING CHARACTERISTICS**					
$t_{d(on)}$	Turn-On Delay Time		3.0	ns	$V_{DD} = 10$ Vdc, $I_{D(on)} = 10$ mAdc, $V_{GS(on)} = 10$ Vdc, $V_{GS(off)} = 0$, $R_G = 50$ Ohms
t_r	Rise Time		10	ns	
$t_{d(off)}$	Turn-Off Delay Time		3.0	ns	
t_f	Fall Time		15	ns	

*Indicates JEDEC Registered Data.

DIODE PROTECTED P-CHANNEL ENHANCEMENT MODE MOS FET

3N172

FEATURES

- High Input Impedance
- Diode Protected Gate

MAXIMUM RATINGS

(@25°C ambient unless noted)

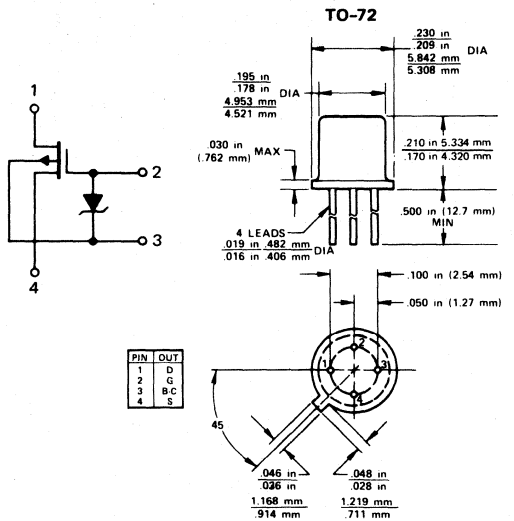
		3N172
V_{GSS}	Gate to Source Voltage	-40 V
V_{DSS}	Drain to Source Voltage	-40 V
V_{SDS}	Source to Drain Voltage	-40 V
V_{DGO}	Drain to Gate Voltage	-40 V
I_D	Drain Current	-50 mA
$I_{G(f)}$	Gate Forward Current	10 μA
$I_{G(r)}$	Gate Reverse Current	1.0 mA
P_D	Power Dissipation	375 mW
	Derating Factor	3.0 mW/°C
T_j	Operating Junction Temperature	-55 to +150°C
T_{stg}	Storage Temperature	-65 to +200°C
T_l	Lead Temperature 1/16" from Case for 10 sec max	+300°C

ORDERING INFORMATION

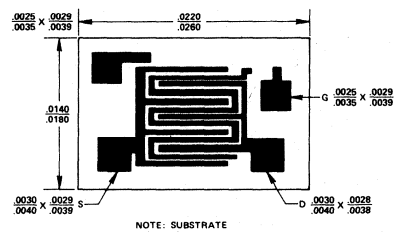
TO72	WAFER	CHIP
3N172	3N172/W	3N172/D

PACKAGE DIMENSIONS

TO-72



1503-Z



NOTE: SUBSTRATE IS BODY.

ELECTRICAL CHARACTERISTICS (@ 25°C and V_{BS} = 0 unless noted)

	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
I_{GSS}	Gate Reverse Current		-200	pA	V_{GS} = -20 V
I_{GSS}	Gate Reverse Current (+125°C)		-0.5	μA	V_{GS} = -20 V
BV_{GSS}	Gate Breakdown Voltage	-40	-125	V	I_D = -10 μA
BV_{DSS}	Drain-Source Breakdown Voltage	-40		V	I_D = -10 μA
BV_{SDS}	Source-Drain Breakdown Voltage	-40		V	I_S = -10 μA, V_{DB} = 0
$V_{GS(th)}$	Threshold Voltage	-2.0	-5.0	V	V_{DS} = V_{GS}, I_D = -10 μA
$V_{GS(th)}$	Threshold Voltage	-2.0	-5.0	V	V_{DS} = -15 V, I_D = -10 μA
V_{GS}	Gate Source Voltage	-3.0	-6.5	V	V_{DS} = -15 V, I_D = -500 μA
I_{DSS}	Zero Gate Voltage Drain Current		-0.4	nA	V_{DS} = -15 V
I_{SDS}	Zero Gate Voltage Source Current		-0.4	nA	V_{SD} = -15 V, V_{DB} = 0
$r_{ds(on)}$	Drain Source On Resistance		250	ohms	V_{GS} = -20 V, I_D = -100 μA
$I_{D(on)}$	On Drain Current	-5.0	-30	mA	V_{DS} = -15 V, V_{GS} = -10 V

FEATURES

- Very High Input Impedance
- Low Capacitance
- High Gate Breakdown 3N190-3N191
- Zener Protected gate 3N188-3N189
- V_g & (TH) Matched
- V_g & (TH) Tracking

Intersil

DUAL MATCHED P-CHANNEL ENHANCEMENT MODE MOS FETS

3N188 3N189 3N190 3N191

MAXIMUM RATINGS
(@ 25°C ambient unless noted)

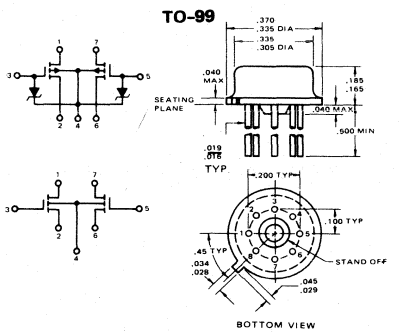
		3N188 3N189	3N190 3N191
V_{GSS}	Static Gate to Source Voltage	±40V	-40V
V_{GSS}[1]	Transient Gate to Source Voltage	±40V	±125V
V_{DSS}	Drain to Source Voltage	-40V	-40V
V_{SDS}	Source to Drain Voltage	-40V	-40V
I_D	Drain Current	50 mA	50 mA
P_D	Power Dissipation (each side)	300 mW	
	(both sides)	525 mW	
	Total Derating Factor	4.2 mW/°C	
T_j	Operating Junction Temperature	-55 to +150°C	
T_{stg}	Storage Temperature	-65 to +200°C	
T_l	Lead Temperature 1/16" from Case for 10 sec max	+300°C	

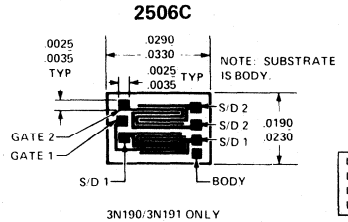
[1] Device must not be tested at b125V more than once or for longer than 300 ms.

ORDERING INFORMATION

TO99	WAFER	CHIP
3N188		
3N189		
3N190	3N190/W	3N190/D
3N191	3N191/W	3N191/D

PACKAGE DIMENSIONS





3N190/3N191 ONLY

LEAD 1 DRAIN 1	LEAD 5 GATE 2
LEAD 2 SOURCE 1	LEAD 6 SOURCE 2
LEAD 3 GATE 1	LEAD 7 DRAIN 2
LEAD 4 BODY	LEAD 8 (NOT CONNECTED)

ALL DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
BODY (SUBSTRATE) INTERNALLY CONNECTED TO METAL CASE

ELECTRICAL CHARACTERISTICS (@ 25°C and V_{BS} = 0 unless noted)

		3N188 3N189 MIN	3N188 3N189 MAX	3N190 3N191 MIN	3N190 3N191 MAX	UNITS	TEST CONDITIONS
I_{GSS}	Gate Reverse Current				10	pA	V_{GS} = 40V
$I_{G(f)}$	Gate Forward Current		-200		-10	pA	V_{GS} = -40V
$I_{G(f)}$	Gate Forward Current @ 125°C		-200		-25	pA	V_{GS} = -40V
BV_{DSS}	Drain-Source Breakdown Voltage	-40		-40		V	I_D = -10μA
BV_{SDS}	Source-Drain Breakdown Voltage	-40		-40		V	I_S = -10μA, V_{BD} = 0
$V_{GS(th)}$	Threshold Voltage	-2.0	-5.0	-2.0	-5.0	V	V_{DS} = -15V, I_D = -10 μA
$V_{GS(th)}$	Threshold Voltage	-2.0	-5.0	-2.0	-5.0	V	V_{DS} = V_{GS}, I_D = -10 μA
V_{GS}	Gate Source Voltage	-3.0	-6.5	-3.0	-6.5	V	V_{DS} = -15V I_D = -500 μA
I_{DSS}	Zero Gate Voltage Drain Current		-200		-200	pA	V_{DS} = -15V
I_{SDS}	Source Drain Current		-400		-400	pA	V_{SD} = -15V, V_{DB} = 0
$r_{ds(on)}$	Drain-Source on Resistance		300		300	ohms	V_{DS} = -20V, I_D = -100 μA
$I_{D(on)}$	On Drain Current	-5.0	-30.0	-5.0	-30.0	mA	V_{DS} = -15V, V_{GS} = -10V
Y_{fs}	Forward Transconductance	1500	4000	1500	4000	μmhos	V_{DS} = -15V, I_D = -5 mA, f = 1 kHz
Y_{OS}	Output Admittance		300		300	μmhos	V_{DS} = -15V, I_D = -5 mA, f = 1 kHz
C_{iss}	Input Capacitance Output Shorted		4.5		4.5	pF	V_{DS} = -15V, I_D = -5 mA, f = 1 MHz
C_{rss}	Reverse Transfer Capacitance		1.5		1.0	pF	V_{DS} = -15V, I_D = -5 mA, f = 1 MHz
C_{oss}	Output Capacitance Input Shorted		3.0		3.0	pF	V_{DS} = -15V, I_D = -5 mA, f = 1 MHz
$R_E(Y_{fs})$	Real Part of Transconductance	1200		1200		μmhos	V_{DS} = -15V, I_D = -5 mA, f = 100 MHz

SWITCHING CHARACTERISTICS (@ 25°C and V_{BS} = 0 unless noted)

		MIN	MAX	UNITS	TEST CONDITIONS
$t_{D(on)}$	Turn On Delay Time		15	ns	V_{DD} = -15V, I_D = -5 mA
t_r	Rise Time		30	ns	R_G = R_L = 1.4 kΩ
t_{off}	Turn Off Time		50	ns	

MATCHING CHARACTERISTICS (@ 25°C and V_{BS} = 0 unless noted) 3N188 and 3N190

		MIN	MAX	UNITS	
Y_{fs1}/Y_{fs2}	Forward Transconductance Ratio	0.85	1.0		V_{DS} = -15V, I_D = -500 μA, f = 1 kHz
V_{GS1-2}	Gate Source Threshold Voltage Differential		100	mV	V_{DS} = -15V, I_D = -500 μA
ΔV_{GS1-2}	Gate Source Threshold Voltage Differential Change with Temperature		8	mV	V_{DS} = -15V, I_D = -500 μA, T = -55°C to + 25°C
$\frac{\Delta V_{GS1-2}}{\Delta T}$	Gate Source Threshold Voltage Differential Change with Temperature		10	mV	V_{DS} = -15V, I_B = -500 μA, T = +25°C to +125°C

Intersil

LOW LEAKAGE
MONOLITHIC
DUAL DIODE

ID100 ID101

FEATURES

- I_R = 0.1 pA (typical)
- BV_R > 30 V
- C_{TR} = 0.75 pF (typical)

GENERAL DESCRIPTION

The ID100 and ID101 are monolithic dual diodes intended for use in applications requiring extremely low leakage currents. Applications include interstage coupling with reverse isolation, signal clipping and clamping and protection of ultra low leakage FET differential dual and operational amplifiers.

ABSOLUTE MAXIMUM RATINGS

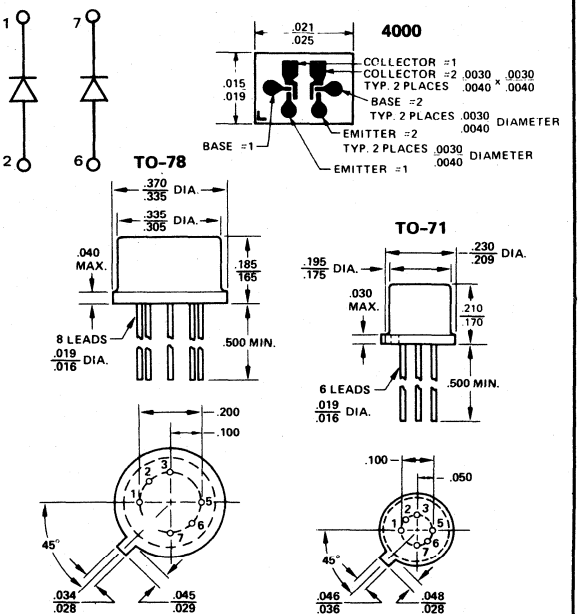
(@ 25°C unless otherwise noted)

Maximum Temperatures	
Storage Temperature	-65°C to +200°C
Operating Junction Temperature	+200°C
Lead Temperature (soldering, 10 sec. time limit)	+300°C
Maximum Power Dissipation	
Device Dissipation @ Free Air Temperature	300 mW
Linear Derating	1.7 mW/°C
Maximum Voltages & Currents	
V_R Reverse Voltage	30 V
$V_{D_1D_2}$ Diode to Diode Voltage	±50 V
I_F Forward Current	20 mA
I_R Reverse Current	100 μA

ORDERING INFORMATION

TO78	TO71	WAFER	CHIP
ID100		ID100/W	ID101/D
	ID101		

PACKAGE DIMENSIONS



1. Cathode 1 5. Not Used*
2. Anode 1 6. Anode 2
3. Not Used* 7. Cathode 2

1. Cathode 1 5. Not Used*
2. Anode 1 6. Anode 2
3. Not Used* 7. Cathode 2

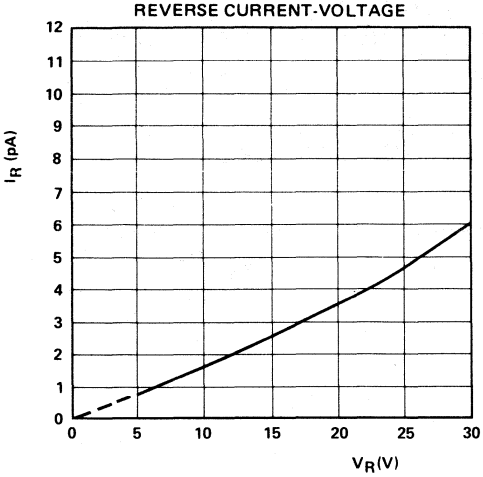
*These leads are not to be connected together nor connected to the circuit in any way.

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

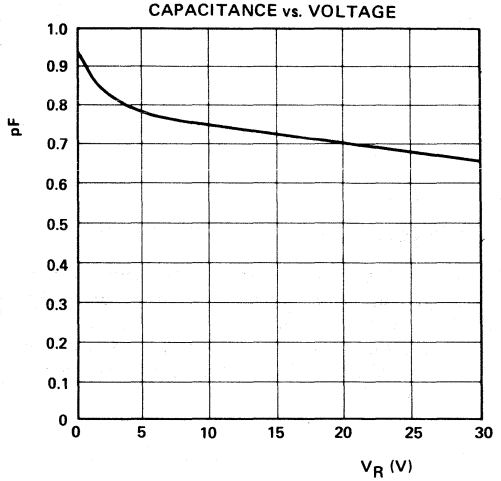
PARAMETER		ID100, ID101 MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
V_F	Forward Voltage Drop	0.8		1.1	V	I_F = 10 mA
BV_R	Reverse Breakdown Voltage	30			V	I_R = 1 μA
I_R	Reverse Leakage Current		0.1		pA	V_R = 1 V, T_A = 25°C
			2.0	10	pA	V_R = 10 V, T_A = 25°C
				10	nA	V_R = 10 V, T_A = 125°C
$\lvert I_{R_1} - I_{R_2} \rvert$	Differential Leakage Current			3	pA	V_R = 10 V
C_{TR}	Total Reverse Capacitance		0.75	1	pF	V_R = 10 V, f = 1 MHz

TYPICAL CHARACTERISTICS OF ID100/ID101

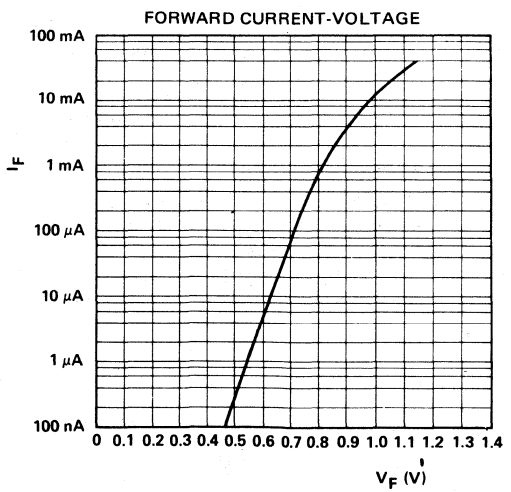
REVERSE CURRENT-VOLTAGE



CAPACITANCE vs. VOLTAGE



FORWARD CURRENT-VOLTAGE



Intersil

LOW NOISE DUAL MONOLITHIC MATCHED N-CHANNEL JFETS

IMF6485

FEATURES

- $\bar{e}_n < 10\,nV/\sqrt{Hz}$ at 10 Hz
- CMRR > 90 dB
- $\Delta |V_{GS1} - V_{GS2}| < 25\,mV$
- $\Delta |V_{GS1} - V_{GS2}| < 40\,\mu V/^\circ C$

GENERAL DESCRIPTION

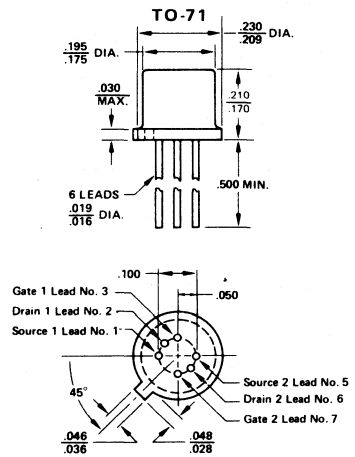
This N-Channel Junction FET is characterized for ultra low noise applications requiring tightly controlled and specified noise parameters at 10 Hz and 1000 Hz. Tight matching specifications make this device ideal as the input stage for low frequency differential instrumentation amplifiers.

ABSOLUTE MAXIMUM RATINGS (Note 1)

(@ 25°C unless otherwise noted)

Maximum Temperatures	
Storage Temperature	-65°C to +150°C
Operating Junction Temperature	+150°C
Lead Temperature (soldering, 10 sec. time limit)	+300°C
Maximum Power Dissipation	
Device Dissipation @ 85°C Free Air Temperature	
One Side	250 mW
Both Sides	500 mW
Linear Derating	
One Side	3.85 mW/°C
Both Sides	7.7 mW/°C
Maximum Voltages & Currents	
V_{GS} Gate to Source Voltage	-50 V
V_{GD} Gate to Drain Voltage	-50 V
$V_{G1\,G2}$ Gate to Gate Voltage	±50 V
I_G Gate Current	50 mA

PACKAGE DIMENSIONS



5019

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise specified)

SYMBOL	CHARACTERISTICS	MIN.	MAX.	UNIT	TEST CONDITIONS
I_{GSS}	Gate Reverse Current		-200	pA	V_{GS} = -30 V, V_{DS} = 0, T_A = +25°C
			-200	nA	V_{GS} = -30 V, V_{DS} = 0, T_A = +150°C
BV_{GSS}	Gate-Source Breakdown Voltage	-50		V	I_G = -1 μA, V_{DS} = 0
V_p	Gate-Source Pinch-Off Voltage	-0.7	-4.0	V	V_{DS} = 20 V, I_D = 1 nA
I_{DSS}	Drain Current at Zero Gate Voltage	0.5	7.5	mA	V_{DS} = 20 V, V_{GS} = 0 (Note 2)
g_{fs}	Common-Source Forward Transconductance	1000	4000	μmho	V_{DS} = 20 V, V_{GS} = 0, f = 1 KHz (Note 2)
g_{oss}	Common-Source Output Conductance		10	μmho	V_{DS} = 20 V, V_{GS} = 0, f = 1 KHz
C_{iss}	Common-Source Input Capacitance		20	pF	V_{DS} = 20 V, V_{GS} = 0, f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		3.5	pF	V_{DS} = 20 V, V_{GS} = 0, f = 1 MHz
I_G	Gate Current		-100	pA	V_{GD} = 20 V, I_D = 200 μA, T_A = +25°C
			-100	nA	V_{DG} = 20 V, I_D = 200 μA, T_A = +150°C
V_{GS}	Gate-Source Voltage	-0.2	-3.8	V	V_{DG} = 20 V, I_D = 200 μA
g_{fs}	Common-Source Forward Transconductance	500	1500	μmho	V_{DG} = 20 V, I_D = 200 μA, f = 1 KHz (Note 2)
g_{os}	Common-Source Output Conductance		1	μmho	V_{DG} = 20 V, I_D = 200 μA
$\bar{e}_n$	Equivalent Input Noise Voltage		15	$nV/\sqrt{Hz}$	V_{DS} = 20 V, I_D = 200 μA, f = 10 Hz
			10	$nV/\sqrt{Hz}$	V_{DS} = 20 V, I_D = 200 μA, f = 1 KHz

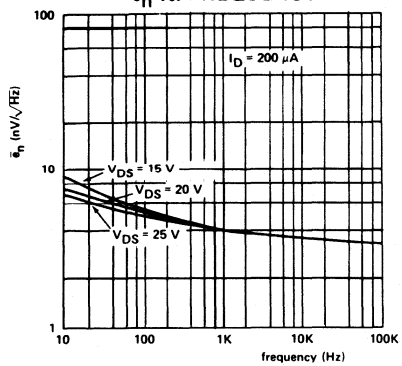
MATCHING CHARACTERISTICS (@ 25° C unless otherwise noted)

SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNIT	CONDITIONS
$\frac{I_{DSS1}}{I_{DSS2}}$	Drain Current Ration at Zero Gate Voltage	0.95	1	–	V_{DS} = 20 V, V_{GS} = 0 (Note 2)
$\lvert I_{G1} - I_{G2} \rvert$	Differential Gate Current		10	nA	V_{DG} = 20 V, I_D = 200 μA T_A = +125° C
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio	0.95	1	–	V_{DG} = 20 V, I_D = 200 μA, f = 1 KHz (Note 2)
$\lvert g_{os1} - g_{os2} \rvert$	Differential Output Conductance		0.1	μmho	V_{DG} = 20 V, I_D = 200 μA, f = 1 KHz
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage		25	mV	V_{DG} = 20 V, I_D = 200 μA
$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift		40	μV/° C	V_{CG} = 20 V, I_D = 200 μA T_A = +25° C to +125° C
$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift		40	μV/° C	V_{DG} = 20 V, I_D = 200 μA T_A = -55° C to +25° C
CMRR	Common Mode Rejection Ratio	90		dB	V_{DD} = 10 to 20 V, I_D = 200 μA (Note 3)

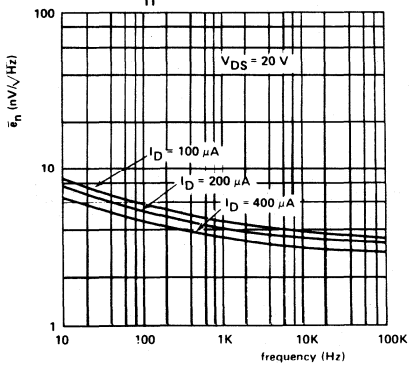
NOTES: 1. These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
2. Pulse duration of 2 ms used during test.
3. CMRR = $20\text{Log}_{10}\Delta V_{DD}/\Delta \lvert V_{GS1} - V_{GS2} \rvert$, ($\Delta V_{DD}$ = 10 V)

TYPICAL CHARACTERISTICS

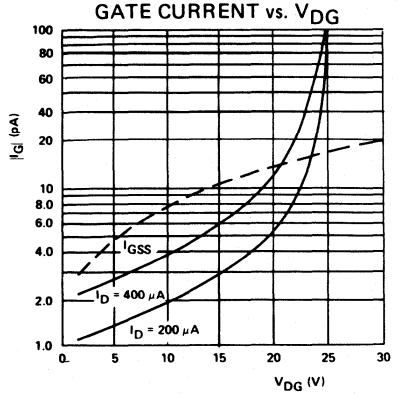
$\bar{e}_n$ vs. FREQUENCY



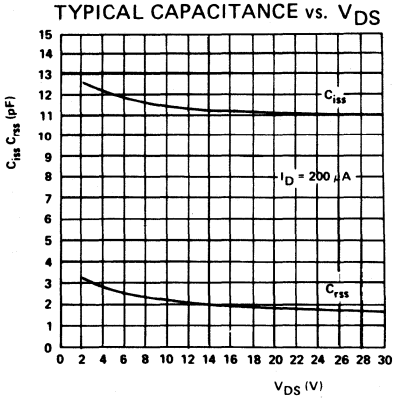
$\bar{e}_n$ vs. FREQUENCY



GATE CURRENT vs. V_{DG}



TYPICAL CAPACITANCE vs. V_{DS}



Intersil

P–CHANNEL SILICON PLANAR EPITAXIAL J FET ANALOG SWITCHES

IT100 IT101

FEATURES

- Interfaces Directly with T^2L Logic Elements so that No Extra Driver Stage is Required.
- $R_{DS(ON)} < 75\Omega$ for 5 V Logic Drive
- $I_{D(OFF)} < 100$ pA

GENERAL DESCRIPTION

This P-channel JFET has been designed to directly interface with T^2L logic, thus eliminating the need for costly drivers, in analog gate circuitry. Bipolar inputs of ±15 V can be switched. The FET is OFF for hi level inputs (+5 V or +15 V) and ON for low level inputs (< 0.5 V for IT100 < 1.5 V for IT101.

ABSOLUTE MAXIMUM RATINGS

@25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature (TO18)	-65°C to +200°C
Storage Temperature (TO92)	-55°C to +125°C
Operating Junction Temperature (TO18)	+200°C
Operating Junction Temperature (TO92)	+125°C
Lead Temperature (Soldering, 10 sec time limit)	+300°C

Maximum Power Dissipation

Device Dissipation @ Free Air Temperature	300 mW
Linear Derating (TO18)	1.7 mW/°C
(TO92)	3.0 mW/°C

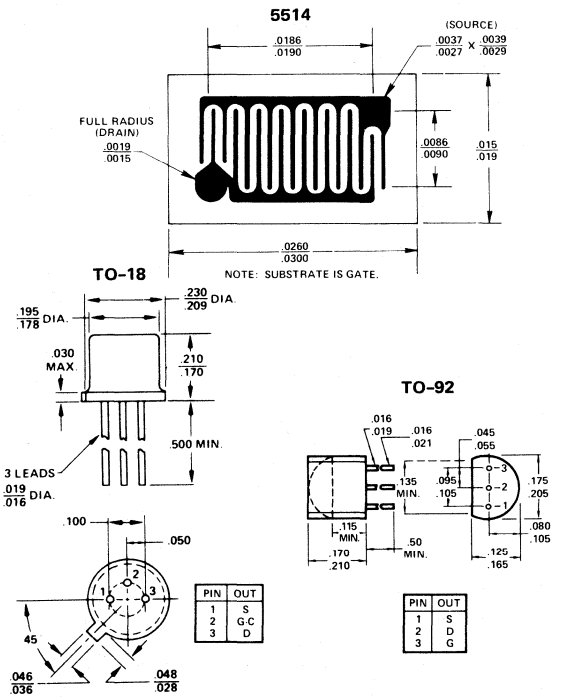
Maximum Voltages & Current

V_{GS}	Gate to Source Voltage	35V
V_{GD}	Gate to Drain Voltage	35V
I_G	Gate Current	50 mA

ORDERING INFORMATION

TO18	TO92	WAFER FORM	CHIP
IT100	IT100-TO92	IT100/W	IT100/D
IT101	IT101-TO92	IT101/W	IT101/D

PACKAGE DIMENSIONS



ELECTRICAL CHARACTERISTICS @25°C (unless otherwise noted)

	CHARACTERISTIC	IT100 MIN	IT100 MAX	IT101 MIN	IT101 MAX	UNIT	TEST CONDITIONS
I_{DSS}	Max Drain Current	-10	–	-20	–	mA	V_{GS} = 0, V_{DS} = -15 V
V_P	Pinch Off Voltage	2	4.5	4	10	V	I_D = 1 nA, V_{DS} = -15 V
BV_{GSS}	Gate-Source Breakdown Voltage	35		35		V	I_G = 1 μA, V_{DS} = 0
I_{GSS}	Gate Leakage Current		200		200	pA	V_{GS} = 20 V, V_{DS} = 0
g_{fs}	Transconductance	-8		-8		mmho	V_{GS} = 0, V_{DS} = -15 V
g_{os}	Output Conductance		-1		-1	mmho	V_{GS} = 0, V_{DS} = -15 V
$I_{D(OFF)}$	Drain (OFF) Leakage		-100		-100	pA	V_{DS} = 10 V, V_{GS} = -15 V
$R_{DS(ON)}$	Drain-Source "ON" Resistance		75		60	Ω	V_{GS} = 0, V_{DS} = -0.1 V
C_{iss}	Input Capacity		35		35	pF	V_{DG} = -20 V, V_{GS} = 0
C_{rss}	Reverse Transfer Capacity		12		12	pF	V_{DG} = -10 V, I_S = 0

FEATURES

- High h_{FE} at Low Current >200 @ 10 μA
- Low Output Capacitance <2.0 pf
- $I_{B1} - I_{B2}$ <2.5 nA
- Tight V_{BE} Tracking <3.0 $\mu V/^{\circ}C$

Intersil

DUAL MONOLITHIC MATCHED NPN SILICON PLANAR TRANSISTORS

IT120A IT120 IT121 IT122

GENERAL DESCRIPTION

Matched pairs for differential amplifiers.

ABSOLUTE MAXIMUM RATINGS (Note 1)

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+200°C

Maximum Power Dissipation

	TO-78		TO-71	
	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Total Dissipation at 25°C Case Temperature	0.4 Watt	0.75 Watt	0.3 Watt	0.5 Watt
Derating Factor	2.3mW/°C	4.3mW/°C	1.7mW/°C	4.3mW/°C

Maximum Voltage & Current for Each Transistor

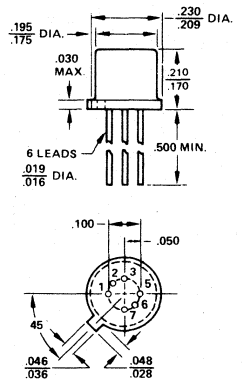
V_{CBO}	Collector to Base Voltage	45 V
V_{CEO}	Collector to Emitter Voltage	45 V
V_{EBO}	Emitter to Base Voltage	7.0 V
V_{CCO}	Collector to Collector Voltage	60 V
I_C	Collector Current	50mA

ORDERING INFORMATION

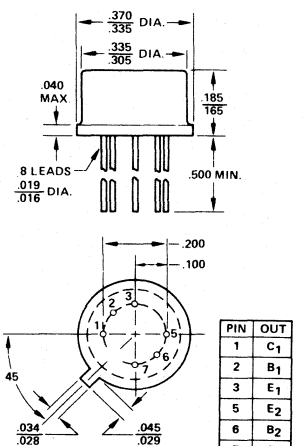
TO78	TO71	WAFER	CHIP
IT120A	IT120A-TO71	IT120A/W	IT120A/D
IT120	IT120-TO71	IT120/W	IT120/D
IT121	IT121-TO71	IT121/W	IT121/D
IT122	IT122-TO71	IT122/W	IT122/D

PACKAGE DIMENSIONS

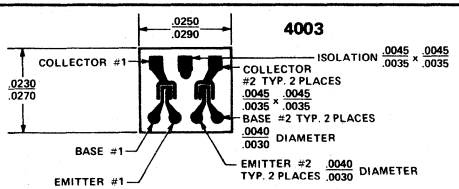
TO-71



TO-78



PIN	OUT
1	C_1
2	B_1
3	E_1
5	E_2
6	B_2
7	C_2



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		IT120A MIN	IT120A MAX	IT120 MIN	IT120 MAX	IT121 MIN	IT121 MAX	IT122 MIN	IT122 MAX	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	200		200		80		80			I_C = 10 μA, V_{CE} = 5.0 V
h_{FE}	DC Current Gain	225		225		100		100			I_C = 1.0 mA, V_{CE} = 5.0 V
h_{FE}(−55°C)	DC Current Gain	75		75		30		30			I_C = 10 μA, V_{CE} = 5.0 V
V_{BE}(ON)	Emitter-Base On Voltage		0.7		0.7		0.7		0.7	V	I_C = 10 μA, V_{CE} = 5.0 V
V_{CE}(SAT)	Collector Saturation Voltage		0.5		0.5		0.5		0.5	V	I_C = 0.5 mA, I_B = 0.05 mA
I_{CBO}	Collector Cutoff Current		1.0		1.0		1.0		1.0	nA	I_E = 0, V_{CB} = 45 V
I_{CBO}(+150°C)	Collector Cutoff Current		10		10		10		10	μA	I_E = 0, V_{CB} = 45 V
I_{EBO}	Emitter Cutoff Current		1.0		1.0		1.0		1.0	nA	I_C = 0, V_{EB} = 5.0 V
C_{OB}	Output Capacitance		2.0		2.0		2.0		2.0	pF	I_E = 0, V_{CB} = 5.0 V
C_{TE}	Emitter Transition Capacitance		2.5		2.5		2.5		2.5	pF	I_C = 0, V_{EB} = 0.5 V
C_{C_1, C_2}	Collector to Collector Capacitance		4.0		4.0		4.0		4.0	pF	V_{CC} = 0
I_{C_1, C_2}	Collector to Collector Leakage Current		10		10		10		10	nA	V_{CC} = ±60 V
V_{CEO}(SUST)	Collector to Emitter Sustaining Voltage	45		45		45		45		V	I_C = 1.0 mA, I_B = 0
f_T	Current Gain	10		10		7		7		MHz	I_C = 10 μA, V_{CE} = 5 V
	Bandwidth Product	220		220		180		180		MHz	I_C = 1 mA, V_{CE} = 5 V
$\lvert V_{BE_1} - V_{BE_2} \rvert$	Base Emitter Voltage Differential		1		2		3		5	mV	I_C = 10 μA, V_{CE} = 5.0 V
$\lvert I_{B_1} - I_{B_2} \rvert$	Base Current Differential		2.5		5		25		25	nA	I_C = 10 μA, V_{CE} = 5.0 V
$\lvert \Delta(V_{BE_1} - V_{BE_2}) \rvert$	Base-Emitter Voltage Differential Change with Temperature		3		5		10		20	$\mu V/^{\circ}C$	T_A = −55°C to +125°C, I_C = 10 μA, V_{CE} = 5.0 V

NOTES:

(1) These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

(2) The lowest of two h_{FE} readings is taken as h_{FE_1} for purposes of this ratio.

Intersil

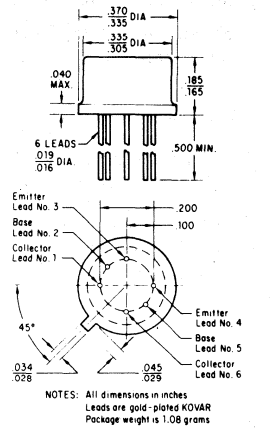
SUPER-BETA DUAL MONOLITHIC NPN SILICON PLANAR TRANSISTORS

IT124

FEATURES

- Very High Gain – $h_{FE} \geq 1500$ @ 1 and 10μA
- Low Output Capacitance – $C_{obo} \leq 0.8$ pF
- Tight V_{BE} Matching – $|V_{BE_1} - V_{BE_2}| - 2$ mV TYP.
- High f_T – 100 MHz

PACKAGE DIMENSIONS



NOTES: All dimensions in inches
Leads are gold-plated KOVAR
Package weight is 1.08 grams

4000

ABSOLUTE MAXIMUM RATINGS (Note 1)

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	-65°C to +200°C
Operating Junction Temperature	+200°C
Lead Temperature (soldering, 10 second time limit)	+300°C

Maximum Power Dissipation

	ONE SIDE	BOTH SIDES
Device Dissipation @ Free Air	400 mW	750 mW
Linear Derating Factor	2.3 mW/°C	4.3 mW/°C

Maximum Voltage and Current for Each Transistor

V_{CBO}	Collector to Base Voltage	2V
V_{CEO}	Collector to Emitter Voltage	2V
V_{EBO}	Emitter to Base Voltage (Note 2)	7V
V_{CCO}	Collector to Collector Voltage	100V
I_C	Collector Current	10mA

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTICS	MIN	MAX	UNITS	CONDITIONS
h_{FE}	DC Current Gain	1500			$I_C = 1\mu A$, $V_{CE} = 1V$
h_{FE}	DC Current Gain	1500			$I_C = 10\mu A$, $V_{CE} = 1V$
h_{FE} (-55°C)	DC Current Gain	600			$I_C = 10\mu A$, $V_{CE} = 1V$
V_{BE} (ON)	Emitter-Base "ON" Voltage		0.7	V	$I_C = 10\mu A$, $V_{CE} = 1V$
V_{CE} (SAT)	Collector Saturation Voltage		0.5	V	$I_C = 1mA$, $I_B = 0.1mA$
I_{CBO}	Collector Cutoff Current		100	pA	$I_E = 0$, $V_{CB} = 1V$
I_{CBO} (+150°C)	Collector Cutoff Current		100	nA	$I_E = 0$, $V_{CB} = 1V$
I_{EBO}	Emitter Cutoff Current		100	pA	$I_C = 0$, $V_{EB} = 5V$
C_{OBO}	Output Capacitance		0.8	pF	$I_E = 0$, $V_{CB} = 1V$
C_{TE}	Emitter Transition Capacitance		1.0	pF	$I_C = 0$, $V_{EB} = 0.5V$
$C_{C_1C_2}$	Collector to Collector Capacitance		0.8	pF	$V_{CC} = 0$
$I_{C_1C_2}$	Collector to Collector Leakage Current		5	pA	$V_{CC} = \pm 100V$
f_T	Current Gain Bandwidth Product	10		MHz	$I_C = 10\mu A$, $V_{CE} = 1V$
f_T	Current Gain Bandwidth Product	100		MHz	$I_C = 200\mu A$, $V_{CE} = 1V$
NF	Narrow Band Noise Figure		3	dB	$I_C = 10\mu A$, $V_{CE} = 3V$, f = 1 KHz, $R_G = 10$ Kohms, BW = 200 Hz
BV_{CBO}	Collector-Base Breakdown Voltage	2		V	$I_C = 10\mu A$, $I_E = 0$
BV_{EBO}	Emitter-Base Breakdown Voltage	7		V	$I_E = 10\mu A$, $I_C = 0$
V_{CEO} (SUST)	Collector-Emitter Sustaining Voltage	2		V	$I_C = 1mA$, $I_B = 0$

MATCHING CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTICS	TYP	MAX	UNITS	CONDITIONS
$\|V_{BE_1} - V_{BE_2}\|$	Base Emitter Voltage Differential	2	5	mV	$I_C = 10\mu A$, $V_{CE} = 1V$
$\|(V_{BE_1} - V_{BE_2})\|/°C$	Base Emitter Voltage Differential Change with Temperature	5	15	μV/°C	$I_C = 10\mu A$, $V_{CE} = 1V$ T = -55°C to +125°C
$\|I_{B_1} - I_{B_2}\|$	Base Current Differential		0.6	nA	$T_C = 10\mu A$, $V_{CE} = 1V$

NOTES:
1. These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.
2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed 10 μAmps.

FEATURES

- High Gain at Low Current – $h_{FE} \geq 230$ at 10 mA -5V
- Low Output Capacitance – $C_{obo} \leq 3$ pF
- Tight I_B Match – $I_{B1-2} < .25\ \mu A$ at 1 mA -5V
- Tight V_{BE} Tracking – $\Delta(V_{BE_1} - V_{BE_2}) \leq 3\ \mu V/°C$ -55°C to +125°C
- Dielectrically isolated matched pairs for differential amplifiers.

Intersil

DUAL MONOLITHIC NPN SILICON PLANAR TRANSISTORS

IT126 IT127 IT128 IT129

GENERAL DESCRIPTION

Dual monolithic NPN Silicon planar transistors used for differential amplifier applications.

ORDERING INFORMATION

TO78	TO71	WAFER	CHIP
IT126	IT126-TO71	IT126/W	IT126/D
IT127	IT127-TO71	IT127/W	IT127/D
IT128	IT128-TO71	IT128/W	IT128/D
IT129	IT129-TO71	IT128/W	IT128/D

ABSOLUTE MAXIMUM RATINGS (Note 1)

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature −65°C to +200°C

Operating Junction Temperature +200°C

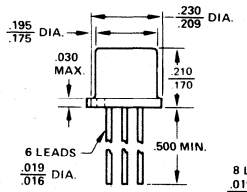
	TO71		TO78	
Maximum Power Dissipation	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Total Dissipation at 25°C Case Temperature	0.3 Watt	0.5 Watt	0.4 Watt	0.75 Watt
Derating Factor	1.7 mW/°C	2.9 mW/°C	2.3 mW/°C	4.3 mW/°C

Maximum Voltage and Current for Each Transistor

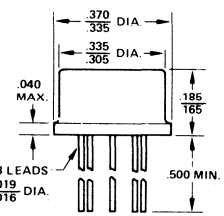
V_{CBO}	Collector to Base Voltage	60V	55V	45V
V_{CEO}	Collector to Emitter Voltage	60V	55V	45V
V_{EBO}	Emitter to Base Voltage (Note 2)	7V	7V	7V
V_{CCO}	Collector to Collector Voltage	70V	70V	70V
I_C	Collector Current	100 mA	100 mA	100 mA

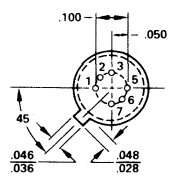
PACKAGE DIMENSIONS

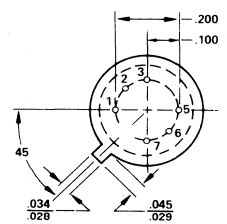
TO-71



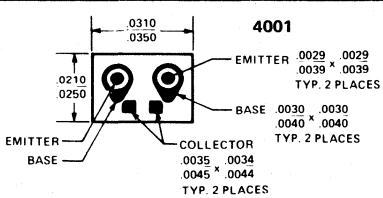
TO-78







1. Collector
2. Base
3. Emitter
5. Emitter
6. Base
7. Collector



ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

PARAMETER		IT126 MIN	IT126 MAX	IT127 MIN	IT127 MAX	IT128 MIN	IT128 MAX	IT129 MIN	IT129 MAX	UNITS	CONDITIONS
h_{FE}	DC Current Gain	150		150		100		70			$I_C = 10\ \mu A$, $V_{CE} = 5V$
h_{FE}	DC Current Gain	200	800	200	800	150	800	100			$I_C = 1.0$ mA, $V_{CE} = 5V$
h_{FE}	DC Current Gain	230		230		170		115			$I_C = 10$ mA, $V_{CE} = 5V$
h_{FE}	DC Current Gain	100		100		75		50			$I_C = 50$ mA, $V_{CE} = 5V$
h_{FE}(-55°C)	DC Current Gain	75		75		60		40			$I_C = 1$ mA, $V_{CE} = 5V$
$V_{BE(on)}$	Emitter-Base On Voltage		.9		.9		.9		.9	V	$I_C = 10$ mA, $V_{CE} = 5V$
			1.0		1.0		1.0		1.0	V	$I_C = 50$ mA, $V_{CE} = 5V$
$V_{CE(sat)}$	Collector Saturation Voltage		.3		.3		.3		.3	V	$I_C = 10$ mA, $I_B = 1$ mA
			.6		.6		.6		.6	V	$I_C = 50$ mA, $I_B = 5$ mA
I_{CBO}	Collector Cutoff Current		0.1		0.1		0.1		0.1*	nA	$I_E = 0$, $V_{CB} = 45V$, 30V*
I_{CBO}(+150°C)	Collector Cutoff Current		0.1		0.1		0.1		0.1*	μA	$I_E = 0$, $V_{CB} = 45V$, 30V*
I_{EBO}	Emitter Cutoff Current		0.1		0.1		0.1		0.1	nA	$I_C = 0$, $V_{EB} = 5V$
C_{obo}	Output Capacitance		3		3		3		3	pF	$I_E = 0$, $V_{CB} = 20V$

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

PARAMETER		IT126		IT127		IT128		IT129		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$BV_{C_1C_2}$	Collector to Collector Breakdown Voltage	100		100		100		100		V	$I_C = \pm 1\ \mu A$
$V_{CEO(sust)}$	Collector to Emitter Sustaining Voltage	60		60		55		45		V	$I_C = 1$ mA, $I_B = 0$
BV_{CBO}	Collector Base Breakdown Voltage	60		60		55		45		V	$I_C = 10\ \mu A$, $I_E = 0$
BV_{EBO}	Emitter Base Breakdown Voltage	7		7		7		7		V	$I_E = 10\ \mu A$, $I_C = 0$

MATCHING CHARACTERISTICS @ 25°C (unless otherwise noted)

PARAMETER		IT126		IT127		IT128		IT129		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$\lvert V_{BE_1} - V_{BE_2} \rvert$	Base Emitter Voltage Differential		1		2		3		5	mV	$I_C = 1$ma , $V_{CE} = 5V$
$\lvert \Delta(V_{BE_1} - V_{BE_2}) \rvert / °C$	Base-Emitter Voltage Differential Change with Temperature		3		5		10		20	$\mu V/°C$	$I_C = 1$ mA, $V_{CE} = 5V$ $T_A = -55°C$ to $+125°C$
$\lvert I_{B_1} - I_{B_2} \rvert$	Base Current Differential		2.5		5		10		20	nA	$I_C = 10\ \mu A$, $V_{CE} = 5V$
			.25		.5		1.0		2.0	μA	$I_C = 1$ mA, $V_{CE} = 5V$

FEATURES

- High h_{FE} at Low Current >200 @ 10 μA
- Low Output Capacitance <2.0 pf
- $I_{B1} - I_{B2} < 2.5$ nA
- Tight V_{BE} Tracking $<3.0\ \mu V/^{\circ}C$

GENERAL DESCRIPTION

Matched pairs for differential amplifiers.

Intersil

DUAL MONOLITHIC MATCHED PNP SILICON PLANAR TRANSISTORS

IT130A IT130 IT131 IT132

ABSOLUTE MAXIMUM RATINGS (Note 1)

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	-65°C to +200°C
Operating Junction Temperature	+200°C

Maximum Power Dissipation

	TO-78		TO-71	
	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Total Dissipation at 25°C Case Temperature	0.4 Watt	0.75 Watt	0.3 Watt	0.5 Watt
Derating Factor	2.3mW/°C	4.3mW/°C	1.7mW/°C	2.9mW/°C

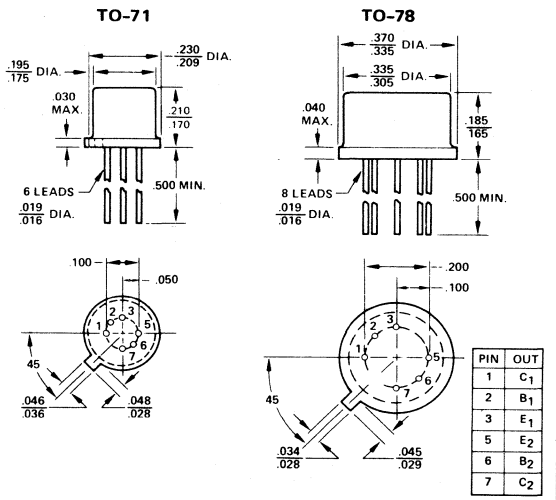
Maximum Voltage & Current for Each Transistor

V_{CBO}	Collector to Base Voltage	45 V
V_{CEO}	Collector to Emitter Voltage	45 V
V_{EBO}	Emitter to Base Voltage	7.0 V
V_{CCO}	Collector to Collector Voltage	60 V
I_C	Collector Current	50 mA

ORDERING INFORMATION

TO78	TO71	WAFER	CHIP
IT130A	IT130A-TO71	IT130A/W	IT130A/D
IT130	IT130-TO71	IT130/W	IT130/D
IT131	IT131-TO71	IT131/W	IT131/D
IT132	IT132-TO71	IT132/W	IT132/D

PACKAGE DIMENSIONS



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		IT130A		IT130		IT131		IT132		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
h_{FE}	DC Current Gain	200		200		80		80			I_C = 10 μA, V_{CE} = 5.0 V
h_{FE}	DC Current Gain	225		225		100		100			I_C = 1.0 mA, V_{CE} = 5.0 V
h_{FE}(-55°C)	DC Current Gain	75		75		30		30			I_C = 10 μA, V_{CE} = 5.0 V
V_{BE}(ON)	Emitter-Base On Voltage		0.7		0.7		0.7		0.7	V	I_C = 10 μA, V_{CE} = 5.0 V
V_{CE}(SAT)	Collector Saturation Voltage		0.5		0.5		0.5		0.5	V	I_C = 0.5 mA, I_B = 0.05 mA
I_{CBO}	Collector Cutoff Current		-1.0		-1.0		-1.0		-1.0	nA	I_E = 0, V_{CB} = 45 V
I_{CBO}(+150°C)	Collector Cutoff Current		-10		-10		-10		-10	μA	I_E = 0, V_{CB} = 45 V
I_{EBO}	Emitter Cutoff Current		-1.0		-1.0		-1.0		-1.0	nA	I_C = 0, V_{EB} = 5.0 V
C_{OB}	Output Capacitance		2.0		2.0		2.0		2.0	pF	I_E = 0, V_{CB} = 5.0 V
C_{TE}	Emitter Transition Capacitance		2.5		2.5		2.5		2.5	pF	I_C = 0, V_{EB} = 0.5 V
C_{C_1, C_2}	Collector to Collector Capacitance		4.0		4.0		4.0		4.0	pF	V_{CC} = 0
I_{C_1, C_2}	Collector to Collector Leakage Current		10		10		10		10	nA	V_{CC} = ±60 V
V_{CEO}(SUST)	Collector to Emitter Sustaining Voltage	-45		-45		-45		-45		V	I_C = 1.0 mA, I_B = 0
f_T	Current Gain	5		5		4		4		MHz	I_C = 10 μA, V_{CE} = 5 V
	Bandwidth Product	110		110		90		90		MHz	I_C = 1 mA, V_{CE} = 5 V
$\lvert V_{BE_1} - V_{BE_2} \rvert$	Base Emitter Voltage Differential		1		2		3		5	mV	I_C = 10 μA, V_{CE} = 5.0 V
$\lvert I_{B_1} - I_{B_2} \rvert$	Base Current Differential		2.5		5		25		25	nA	I_C = 10 μA, V_{CE} = 5.0 V
$\lvert \Delta(V_{BE_1} - V_{BE_2}) \rvert$	Base-Emitter Voltage Differential Change with Temperature		3		5		10		20	$\mu V/^{\circ}C$	T_A = -55°C to +125°C, I_C = 10 μA, V_{CE} = 5.0 V

NOTES:

(1) These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

(2) The lowest of two h_{FE} readings is taken as h_{FE_1} for purposes of this ratio.

FEATURES

- High Gain at Low Current – $h_{FE} \geq 200$ @ 1mA
- Low Output Capacitance – $C_{obo} < 3$ pf
- Tight I_B Match – $I_{B_1 - 2} < .25\ \mu A$ @ 1 mA – 5V
- Tight V_{BE} Tracking – $\Delta(V_{BE_1} - V_{BE_2}) \leq 3\ \mu V/°C$ −55°C to + 125°C
- Dielectrically isolated matched pairs for differential amplifiers.

Intersil

DUAL MONOLITHIC PNP SILICON PLANAR TRANSISTORS

IT136 IT137 IT138 IT139

GENERAL DESCRIPTION

Dual monolithic PNP silicon planar transistors used for differential amplifier applications.

ABSOLUTE MAXIMUM RATINGS (Note 1)

@ 25°C (unless otherwise noted)

Maximum Temperatures

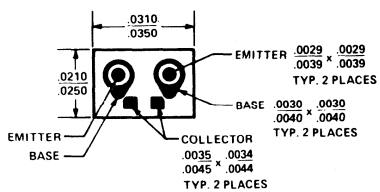
Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+200°C

Maximum Power Dissipation

	TO71		TO78	
	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Total Dissipation @ 25°C				
Case Temperature	0.3 Watt	0.5 Watt	0.4 Watt	0.75 Watt
Derating Factor	1.7mW/°C	2.9mW/°C	2.3mW/°C	4.3mW/°C

Maximum Voltage and Current for Each Transistor

V_{CBO}	Collector to Base Voltage	60V	55V	45V
V_{CEO}	Collector to Emitter Voltage	60V	55V	45V
V_{EBO}	Emitter to Base Voltage (Note 2)	7V	7V	7V
V_{CCO}	Collector to Collector Voltage	70V	70V	70V
I_C	Collector Current	100mA	100mA	100mA



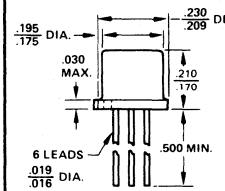
4501

ORDERING INFORMATION

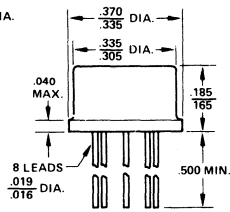
TO78	TO71	WAFER	CHIP
IT136	IT136-TO71	IT136/W	IT136/D
IT137	IT137-TO71	IT137/W	IT137/D
IT138	IT138-TO71	IT138/W	IT138/D
IT139	IT139-TO71	IT139/W	IT139/D

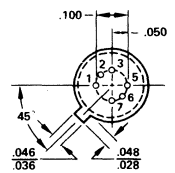
PACKAGE DIMENSIONS

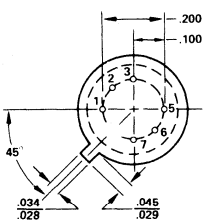
TO-71



TO-78







1. Collector
2. Base
3. Emitter
5. Emitter
6. Base
7. Collector

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

PARAMETER		IT136		IT137		IT138		IT139		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
h_{FE}	DC Current Gain	150		150		100		70			$I_C = 10\ \mu A$, $V_{CE} = 5V$
h_{FE}	DC Current Gain	150	800	150	800	100	800	70	800		$I_C = 1.0$ mA, $V_{CE} = 5V$
h_{FE}	DC Current Gain	125		125		80		50			$I_C = 10$ mA, $V_{CE} = 5V$
h_{FE}	DC Current Gain	65		60		40		25			$I_C = 50$ mA, $V_{CE} = 5V$
$h_{FE}(-55°C)$	DC Current Gain	75		75		60		40			$I_C = 1$ mA, $V_{CE} = 5V$
$V_{BE(on)}$	Emitter - Base On Voltage		.9		.9		.9		.9	V	$I_C = 10$ mA, $V_{CE} = 5V$
			1.0		1.0		1.0		1.0	V	$I_C = 50$ mA, $V_{CE} = 5V$
$V_{CE(sat)}$	Collector Saturation Voltage		.3		.3		.3		.3	V	$I_C = 1$ mA, $I_B = .1$ mA
			.6		.6		.6		.6	V	$I_C = 10$ mA, $I_B = 1$ mA
I_{CBO}	Collector Cutoff Current		0.1		0.1		0.1		0.1*	nA	$I_E = 0$, $V_{CB} = 45V$, 30V*
$I_{CBO}(+150°C)$	Collector Cutoff Current		0.1		0.1		0.1		0.1*	μA	$I_E = 0$, $V_{CB} = 45V$, 30V*
I_{EBO}	Emitter Cutoff Current		0.1		0.1		0.1		0.1	nA	$I_C = 0$, $V_{EB} = 5V$
C_{obo}	Output Capacitance		3		3		3		3	pF	$I_E = 0$, $V_{CB} = 20V$

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

PARAMETERS		IT136		IT137		IT138		IT139		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$BV_{C_1C_2}$	Collector to Collector Breakdown Voltage	100		100		100		100		V	$I_C = \pm 1\ \mu A$
$V_{CEO(sust)}$	Collector to Emitter Sustaining Voltage	60		60		55		45		V	$I_C = 1$ mA, $I_B = 0$
BV_{CBO}	Collector Base Breakdown Voltage	60		60		55		45		V	$I_C = 10\ \mu A$, $I_E = 0$
BV_{EBO}	Emitter Base Breakdown Voltage	7		7		7		7		V	$I_E = 10\ \mu A$, $I_C = 0$

MATCHING CHARACTERISTICS @ 25°C (unless otherwise noted)

PARAMETERS		IT136		IT137		IT138		IT139		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$\lvert V_{BE_1} - V_{BE_2} \rvert$	Base Emitter Voltage Differential		1		2		3		5	mV	$I_C = 1$ ma , $V_{CE} = 5V$
$\lvert \Delta(V_{BE_1} - V_{BE_2}) \rvert / °C$	Base Emitter Voltage Differential Change with Temperature		3		5		10		20	$\mu V/°C$	$I_C = 1$ mA, $V_{CE} = 5V$ $T_A = -55°C$ to $+125°C$
$\lvert I_{B_1} - I_{B_2} \rvert$	Base Current Differential		2.5		5		10		20	nA	$I_C = 10\ \mu A$, $V_{CE} = 5V$
			.25		.5		1.0		2.0	μA	$I_C = 1$ mA, $V_{CE} = 5V$

MONOLITHIC DRIVER DIODE N-CHANNEL JUNCTION FET COMBINATION

IT400

FEATURES

- $R_{DS(on)}$ 25 ohm typ.
- $I_{D(off)}$ of 10 pa typ.
- switching times of 25 ns for t_{on} and 75 ns for t_{off} (R_L = 1K)
- built-in overvoltage protection to plus or minus 25V
- Charge injection of 3 mV typ. into 0.01μf capacitor

GENERAL DESCRIPTION

The IT400 is a monolithically constructed combination of a varactor type Diode and an N-channel Junction Fet. The Fet itself is very similar to the popular 2N4391, and the driver diode is a specially designed diode such that its capacity is a strong function of the voltage across it. The driver diode is electrically in series with the gate of the N-channel Fet and simulates a back to back diode structure; this structure is needed to prevent forward biasing the source to gate or drain to gate junctions of the Fet when used in switching applications.

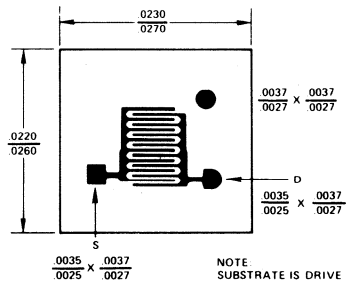
Previous applications of Junction Fets required the addition of diodes, in series with the gate, and then perhaps a gate to source referral resistor or a capacitor in parallel with the diode; therefore at least 3 components were required to perform the switch function. The IT400 does this same job in one component (with a great deal better performance characteristics).

To practically perform a solid state switch function, a translator should be added to drive the diode. This translator takes the T^2L levels and converts them to voltages required to drive the Diode/Fet system (typically a 0V to -15V translation and a 3V to +15V shift. With ±15V power supplies the IT400 will typically switch 14 Vpp at any frequency from dc to 20 MHz.

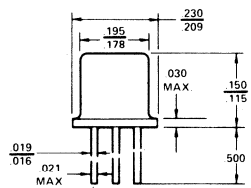
ORDERING INFORMATION

TO52	TO92	WAFER	CHIP
IT400	IT400-TO92	IT400/W	IT400/D

PACKAGE DIMENSIONS



TO-52



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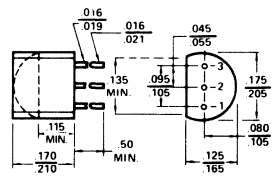
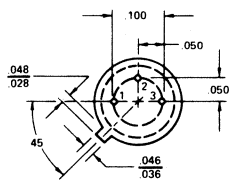




TO-52

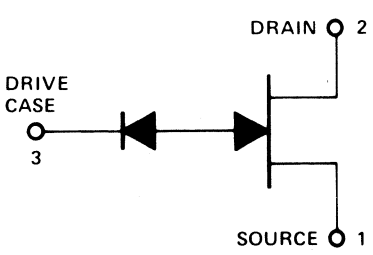
PIN	OUT
1	SOURCE
2	DRAIN
3	DRIVE CASE

TO-92

PIN	OUT
1	SOURCE
2	DRAIN
3	DRIVE

SCHEMATIC DIAGRAM

TO-52



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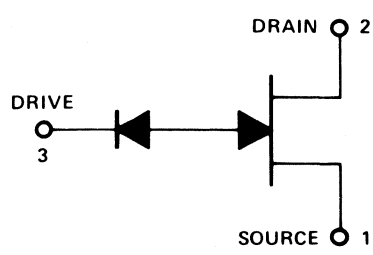
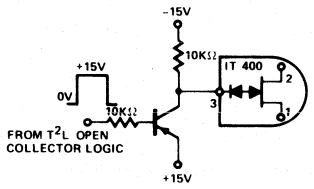


TYPICAL APPLICATIONS

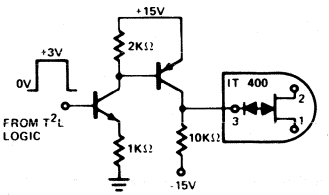
I. Translating from T^2L open collector logic (15V logic) to make a solid state switch.

Have open collector of TTL logic drive directly into 10K base resistor. When logic output is 0V, switch is "on". t_{on} time will be fast but t_{off} time will be limited by storage time of PNP. Base and collector resistors can be adjusted to improve this.



II. Translating from low level T^2L logic to make a solid state switch.

When TTL logic is in "high" state, switch is on. As before t_{on} will be very fast but t_{off} time will be limited by PNP storage. Adjusting 2K and 10K will speed up off time.



APPLICATION TIP

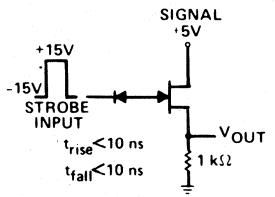
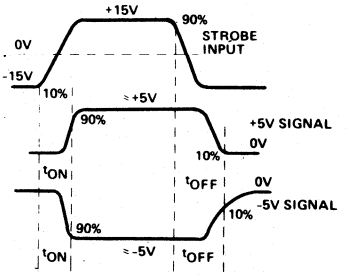


FIGURE A



The ac peak to peak range of 10 Vpp (min. guaranteed but 14 Vpp typical) would seem to be a little restrictive, and this restriction applies when you are switching bipolar signals (i.e. ac signals referred to Gnd.). Actually the IT400 will switch any voltage between minus 7.5V and plus 7.5V, with no problems, as long as the peak to peak amplitude is 10V or less. I.e. −2.5V to +7.5V or −5V to +5V.

Additionally the part will switch up to +10V as long as the input signal is in the 0V to 10V range. In other words the limiting factor, on input voltage handling capability, is signal excursion and not signal absolute voltage. This phenomena is caused by ratio of diode capacity to Fet gate to source capacity.

FEATURES

- High Input Impedance – 10^{15} ohms
- Low Leakage – $I_{DSS} \leq 200$ pA
- Low On-Resistance – $r_{DS(on)} \leq 400$ ohms
- Low Noise Voltage – e_n 150 nV/√Hz typical @ 100 Hz
- High Gain – $Y_{fs} \geq 2000 \leq 4000$ μmhos

P-CHANNEL ENHANCEMENT MODE MOS FET

IT1700

ABSOLUTE MAXIMUM RATINGS (Note 1)

@ 25°C (unless otherwise noted)

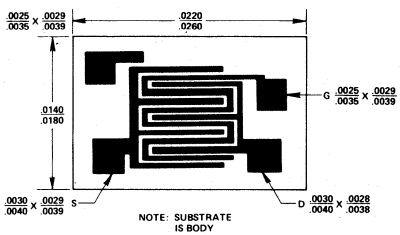
Maximum Temperatures	
Storage Temperature	-65°C to +200°C
Operating Junction Temperature	-55°C to +150°C
Lead Temperature (soldering, 10 second time limit)	+300°C
Maximum Power Dissipation	
Total Dissipation at 25°C Ambient Temperature	0.375 W
Linear Derating Factor at 25°C Ambient Temperature	3 mW/°C
Total Dissipation at 25°C Case Temperature	1.25 W
Linear Derating Factor at 25°C Case Temperature	10 mW/°C
Maximum Voltages and Current	
V_{DSS} Drain to Source and Body Voltage	-40 V
V_{SDS} Source to Drain and Body Voltage	-40 V
V_{GSS} Transient Gate to Source Voltage (Note 2)	±125 V
V_{GSS} Gate to Source Voltage	-40 V
$I_{D(on)}$ Drain Current	50 mA

ORDERING INFORMATION

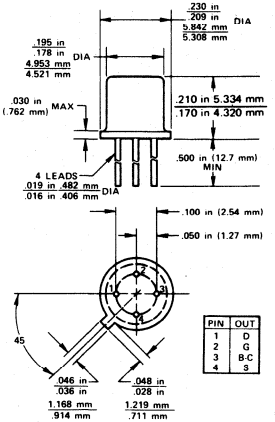
TO72	WAFER	CHIP
IT1700	IT1700/W	IT1700/D

PACKAGE DIMENSIONS

1503



TO-72



ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
BV_{DSS}	Drain to Source Breakdown Voltage	-40		V	V_{GS} = 0, I_D = -10 μA
BV_{SDS}	Source to Drain Breakdown Voltage	-40		V	V_{GS} = 0, I_D = -10 μA
I_{GSS}	Gate Leakage Current				(See Note 2)
I_{DSS}	Drain to Source Leakage Current		200	pA	V_{GS} = 0, V_{DS} = -20 V
I_{DSS} (150°C)	Drain to Source Leakage Current		0.4	μA	V_{GS} = 0, V_{DS} = -20 V
I_{SDS}	Source to Drain Leakage Current		400	pA	V_{GS} = 0, V_{DS} = -20 V
I_{SDS} (150°C)	Source to Drain Leakage Current		0.8	μA	V_{GS} = 0, V_{DS} = -20 V
$V_{GS(th)}$	Gate Threshold Voltage	-2	-5	V	V_{GS} = V_{DS}, I_D = -10 μA

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
$r_{DS(on)}$	Static Drain to Source "on" Resistance			400	ohms	V_{GS} = -10 V, V_{DS} = 0
$I_{DS(on)}$	Drain to Source "on" Current	2			mA	V_{GS} = -10 V, V_{DS} = -15 V
Y_{fs}	Forward Transconductance Common Source	2000		4000	μmhos	V_{DS} = -15 V, I_D = -10 mA f = 1 kHz
C_{iss}	Small Signal, Short Circuit, Common Source, Input Capacitance			5	pF	V_{DS} = -15 V, I_D = -10 mA f = 1 MHz
C_{rss}	Small Signal, Short Circuit, Common Source, Reverse Transfer Capacitance			1.2	pF	V_{DG} = -15 V, I_D = 0 f = 1 MHz
C_{oss}	Small Signal, Short Circuit, Common Source, Output Capacitance			3.5	pF	V_{DS} = -15 V, I_D = -10 mA f = 1 MHz
$\overline{e_n}$	Equivalent Input Noise Voltage		150		nV/√Hz	V_{DS} = -15 V, I_D = -1 mA f = 100 Hz; BW = Hz

NOTE:

1. **These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.**
2. **Actual gate current is immeasurable. Package suppliers are required to guarantee a package leakage of < 10 pA. External package leakage is the dominant mode which is sensitive to both transient and storage environment, which cannot be guaranteed.**

Intersil

N-CHANNEL
ENHANCEMENT
MODE MOS FET

IT1750

FEATURES

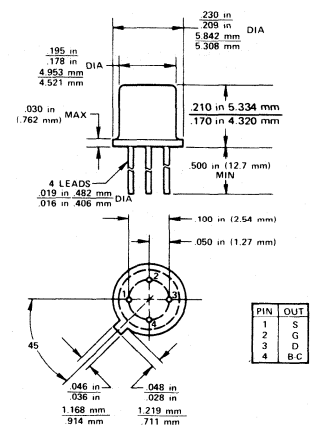
- Low On-Resistance – 50Ω
- Low Capacitance – 1.7 pF
- High Grain – 3,000 μmhos
- High Gate Breakdown Voltage – ±125V
- Low Threshold Voltage – 3 V

ORDERING INFORMATION

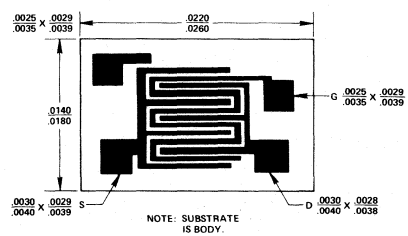
TO72	WAFER	CHIP
IT1750	IT1750/W	IT1750/D

PACKAGE DIMENSIONS

TO-72



1003



ABSOLUTE MAXIMUM RATINGS (Note 1)

@ 25°C (unless otherwise noted)

Maximum Temperatures

Operating Junction Temperature	-55°C to +150°C

Maximum Power Dissipation

Total Dissipation at 25°C Ambient Temp.	0.375 W
Linear Derating Factor at 25°C Ambient Temp.	3 mW/°C

Maximum Voltages and Current

V_{DSS}	Drain to Source and Body Voltage	25 V
V_{GSS}	Transient Gate to Source Voltage	±125 V
$I_{D(on)}$	Drain Current	100 mA

ELECTRICAL CHARACTERISTICS (T_A = 25°C, Body connected to Source unless otherwise noted)

	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
$V_{GS(TH)}$	Gate to Source Threshold Voltage	0.50	1.5	3.0	V	V_{DS} = V_{GS}, I_D = 10 μA, V_{BS} = 0
I_{DSS}	Drain Leakage Current		0.1	10	nA	V_{DS} = 10 V, V_{GS} = V_{BS} = 0
I_{GSS}	Gate Leakage Current					(See Note 2)
BV_{DSS}	Drain Breakdown Voltage	25			V	I_D = 10 μA, V_{GS} = V_{BS} = 0
$R_{DS(on)}$	Drain To Source on Resistance		25	50	ohms	V_{GS} = 20 V, V_{BS} = 0
$I_{D(on)}$	Drain Current	10	50		mA	V_{DS} = V_{GS} = 10 V, V_{BS} = 0
Y_{fs}	Forward Transadmittance	3,000			μmhos	V_{DS} = 10 V, I_D = 10 mA, f = 1 KHz, V_{BS} = 0
C_{iss}	Total Gate Input Capacitance		5.0	6.0	pF	I_D = 10 mA, V_{DS} = 10 V, f = 1 MHz, V_{BS} = 0
C_{dg}	Gate to Drain Capacitance		1.3	1.6	pF	V_{DG} = 10 V, V_{BS} = 0

DIODE PROTECTED N-CHANNEL ENHANCEMENT MODE MOS FET

M116

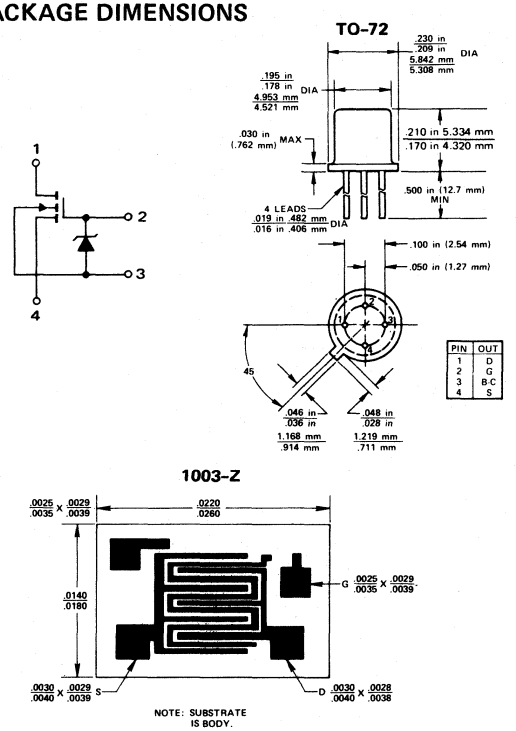
GENERAL DESCRIPTION

- Low I_{GSS}
- Integrated Zener Clamp Protects the Gate

ORDERING INFORMATION

TO72	WAFER	CHIP
M116	M116/W	M116/D

PACKAGE DIMENSIONS



PRODUCT CONDITIONING

Units receive the following treatment before final electrical tests:

High Temp Storage: 24 Hours at 150°C

25,000 Acceleration/Impact in the Y_1 Plane

Thermal Shock: +100 to 0°C for 5 Cycles

Helium and/or Gross Leak Tests for Hermeticity

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-to-Source Voltage	30 V
Gate-to-Drain Voltage	30V
Drain Current	50 mA
Gate Zener Current	±0.1 mA
Storage Temperature	-65 to 150°C
Operating Junction Temperature	-55 to 125°C
Total Device Dissipation (Derate 2.25 mW/°C to 125°C)	225 mW

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		M116 MIN	M116 MAX	TEST CONDITIONS
$r_{DS(on)}$	Drain Source ON Resistance		100 200	V_{GS} = 20 V, I_D = 100 μA, V_{BS} = 0 V_{GS} = 10 V, I_D = 100 μA, V_{BS} = 0
$V_{GS(th)}$	Gate Threshold Voltage	1	5	V_{GS} = V_{DS}, I_D = 10 μA, V_{BS} = 0
BV_{DSS}	Drain-Source Breakdown Voltage	30		I_D = 1 μA, V_{GS} = V_{BS} = 0
BV_{SDS}	Source-Drain Breakdown Voltage	30		I_S = 1 μA, V_{GD} = V_{BD} = 0
BV_{GBS}	Gate-Body Breakdown Voltage	30	60	I_G = 10 μA, V_{SB} = V_{DB} = 0
$I_{D(OFF)}$	Drain Cutoff Current		10	V_{DS} = 20 V, V_{GS} = V_{BS} = 0
$I_{S(OFF)}$	Source Cutoff Current		10	V_{SD} = 20 V, V_{GD} = V_{BD} = 0
I_{GSS}	Gate-Body Leakage		100	V_{GS} = 20 V, V_{DS} = V_{BS} = 0
C_{gs} or C_{gd}	Gate-Source or Gate-Drain Capacitance		2.5	V_{GB} = V_{DB} = V_{SB} = 0, f = 1 MHz Body Guarded
C_{db}	Drain-Body Capacitance		7	V_{GB} = 0, V_{DB} = 10 V, f = 1 MHz
C_{iss}	Input Capacitance		10	V_{GB} = 0, V_{DB} = 10 V, V_{BS} = 0 f = 1 MHz

DUAL MONOLITHIC MATCHED N-CHANNEL JFETS (PAIR)

SU2365 SU2366 SU2367 SU2368 SU2369

FEATURES

- High CMRR
- Low Input Current
- Low Leakage
- Low Noise
- Offset Differential Independent of Operating Current
- Low Offset Differential
- Low Offset Differential With Change in Temperature

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	−65°C to +150°C
Operating Junction Temperature	+150°C
Lead Temperature (Soldering, 10 sec. time limit)	+300°C

Maximum Power Dissipation

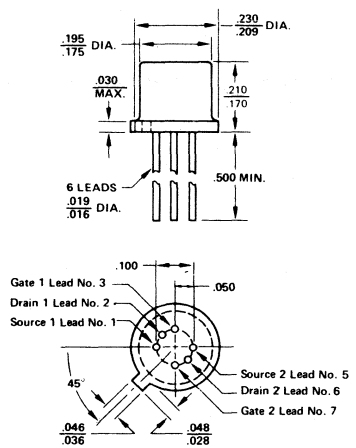
Device Dissipation @ 85°C Free Air Temperature	
One Side	250 mW
Both Sides	500 mW
Linear Derating	
One Side	2.56 mW/°C
Both Sides	4.3 mW/°C

Maximum Voltages & Currents

V_{GS} Gate to Source Voltage	−30 V
V_{GD} Gate to Drain Voltage	−30 V
I_G Gate Current	50 mA

PACKAGE DIMENSIONS

TO-71



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	TEST CONDITIONS	SU2365		SU2366		SU2367		SU2368		SU2369		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$V_{(BR)GSS}$	V_{DS} = 0, I_G = −1.0 μA	−30		−30		−30		−30		−30		V
$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 1.0 nA		−3.5		−3.5		−3.5		−3.5		−3.5	V
V_{GS}	V_{DS} = 15 V, I_D = 200 μA		−2.5		−2.5		−2.5		−2.5		−2.5	V
I_{GSS}	V_{DS} = 0, V_{GS} = −20 V		−100		−100		−100		−100		−100	pA
I_G	V_{DS} = 15 V, I_D = 200 μA, T_A = 25°C		−100		−100		−100		−100		−100	pA
	V_{DS} = 15 V, I_D = 200 μA, T_A = 125°C		−50		−50		−50		−50		−50	nA
I_{DSS}	V_{DS} = 10 V, V_{GS} = 0	0.5	10	0.5	10	0.5	10	0.5	10	0.5	10	mA
g_{fs}	V_{DG} = 15 V, I_D = 200 μA, f = 1.0 KHz	1000	2000	1000	2000	1000	2000	1000	2000	1000	2000	μmhos
g_{fs}	V_{DS} = 10 V, V_{GS} = 0, f = 1.0 KHz	1500		1500		1500		1500		1500		μmhos
g_{os}	V_{DG} = 15 V, I_D = 200 μA		2.0		2.0		2.0		2.0		2.0	μmhos
C_{iss}	V_{DG} = 15 V, I_D = 200 μA, f = 0.14 MHz		16		16		16		16		16	pF
C_{rss}	V_{DG} = 15 V, I_D = 200 μA, f = 0.14 MHz		4.0		4.0		4.0		4.0		4.0	pF
$\overline{e_n}$	V_{DS} = 15 V, V_{GS} = 0, f = 1.0 KHz		50		50		50		50		50	$nV/\sqrt{Hz}$
ΔV_{GS}	ΔV_{DG} = 10-20 V, I_D = 200 μA		0.5		0.5		0.6		0.75		2.0	mV
CMRR	ΔV_{DG} = 10-20 V, I_D = 200 μA	86		86		84		82		74		dB
$\lvert I_{G1}-I_{G2}\rvert$	V_{DG} = 15 V, I_D = 200 μA, T_A = 100°C		5.0		5.0		5.0		5.0		5.0	nA
$\frac{g_{fs1}}{g_{fs2}}$	V_{DG} = 15 V, I_D = 200 μA, f = 1.0 KHz	0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	
$\lvert V_{GS1}-V_{GS2}\rvert$	V_{DG} = 10 V, I_D = 200 μA		5.0		10		10		15		20	mV
$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T_A}$	V_{DG} = 10 V, I_D = 200 μA, T_A = 0°C to 100°C		10		10		25		25		40	μV/°C
$V_{(BR)G1G2}$	V_{DS} = 0, V_{GS} = 0, I_D = ±1 μA	±30		±30		±30		±30		±30		V

DUAL MONOLITHIC MATCHED N-CHANNEL JFETS (PAIR)

SU2365A SU2366A SU2367A SU2368A SU2369A

FEATURES

- High CMRR
- Low Input Current
- Low Leakage
- Low Noise
- Offset Differential Independent of Operating Current
- Low Offset Differential
- Low Offset Differential With Change in Temp.

ABSOLUTE MAXIMUM RATINGS (Note 1)

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	-65°C to +150°C
Operating Junction Temperature	+150°C
Lead Temperature (Soldering, 10 sec. time limit)	+300°C

Maximum Power Dissipation

Device Dissipation @ 85°C Free Air Temperature

One Side	250 mW
Both Sides	500 mW

Linear Derating

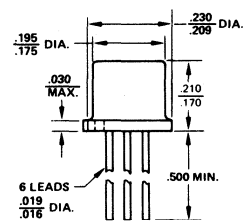
One Side	2.56 mW/°C
Both Sides	4.3 mW/°C

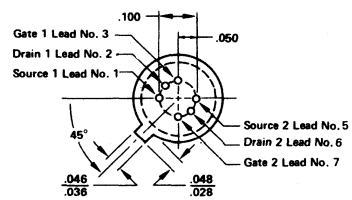
Maximum Voltages & Currents

V_{GS}	Gate to Source Voltage	-30 V
V_{GD}	Gate to Drain Voltage	-30 V
I_G	Gate Current	50 mA

PACKAGE DIMENSIONS

TO-71





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		SU2365A		SU2366A		SU2367A		SU2368A		SU2369A		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$V_{(BR)GSS}$	V_{DS} = 0, I_G = -1.0 μA	-30		-30		-30		-30		-30		V
$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 1.0 nA		-3.5		-3.5		-3.5		-3.5		-3.5	V
V_{GS}	V_{DS} = 15 V, I_D = 200 μA		-2.5		-2.5		-2.5		-2.5		-2.5	V
I_{GSS}	V_{DS} = 0, V_{GS} = -20 V		-50		-50		-50		-50		-50	pA
I_G	V_{DS} = 15 V, I_D = 200 μA, T_A = 25°C		-20		-20		-20		-20		-20	pA
	V_{DS} = 15 V, I_D = 200 μA, T_A = 125°C		-15		-15		-15		-15		-15	nA
I_{DSS}	V_{DS} = 10 V, V_{GS} = 0	0.5	10	0.5	10	0.5	10	0.5	10	0.5	10	mA
g_{fs}	V_{DG} = 15 V, I_D = 200 μA, f = 1.0 KHz	1000	2000	1000	2000	1000	2000	1000	2000	1000	2000	μmhos
g_{fs}	V_{DS} = 10 V, V_{GS} = 0, f = 1.0 KHz	1500		1500		1500		1500		1500		μmhos
g_{os}	V_{DG} = 15 V, I_D = 200 μA		2.0		2.0		2.0		2.0		2.0	μmhos
C_{iss}	V_{DG} = 15 V, I_D = 200 μA, f = 0.14 MHz		16		16		16		16		16	pF
C_{rss}	V_{DG} = 15 V, I_D = 200 μA, f = 0.14 MHz		4.0		4.0		4.0		4.0		4.0	pF
$\overline{e_n}$	V_{DS} = 15 V, V_{GS} = 0, f = 1.0 KHz		15		15		15		15		15	nV/$\sqrt{Hz}$
ΔV_{GS}	ΔV_{DG} = 10-20 V, I_D = 200 μA		0.3		0.3		0.4		0.5		1.0	mV
CMRR	ΔV_{DG} = 10-20 V, I_D = 200 μA		90		90		88		86		80	dB
$\lvert I_{G1}-I_{G2} \rvert$	V_{DG} = 15 V, I_D = 200 μA, T_A = 100°C		0.5		0.5		0.5		0.5		5.0	nA
$\frac{g_{fs1}}{g_{fs2}}$	V_{DG} = 15 V, I_D = 200 μA, f = 1.0 KHz	0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	
$\lvert V_{GS1}-V_{GS2} \rvert$	V_{DG} = 10 V, I_D = 200 μA		5.0		10		10		15		20	mV
$\frac{\Delta \lvert V_{GS1}-V_{GS2} \rvert}{\Delta T_A}$	V_{DG} = 10 V, I_D = 200 μA, T_A = 0°C to 100°C		10		10		25		25		40	μV/°C
$V_{(BR)G1G2}$	V_{DS} = 0, V_{GS} = 0, I_D = ±1 μA	±30		±30		±30		±30		±30		V

DUAL MONOLITHIC MATCHED N-CHANNEL JFETS (PAIR)

U257

GENERAL DESCRIPTION

Matched FET pairs for wideband differential amplifiers.

ORDERING INFORMATION

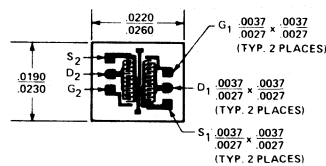
TO99	WAFER	CHIP
U257	U257/W	U257/D

FEATURES

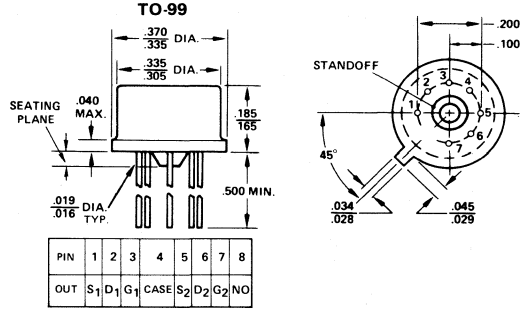
- $g_{fs} > 5000$ μmho from dc to 100 MHz
- Matched V_{GS}, g_{fs} and g_{os}

PACKAGE DIMENSIONS

5022



TO-99



PIN	1	2	3	4	5	6	7	8
OUT	S_1	D_1	G_1	CASE	S_2	D_2	G_2	NO

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Gate-Drain or Gate-Source Voltage	-25 V
Gate Current	50 mA
Device Dissipation (Each Side), T_A = 85°C (Derate 3.85 mW/°C)	250 mW
Total Device Dissipation, T_A = 85°C (Derate 7.7 mW/°C)	500 mW
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		-100	pA	V_{GS} = 15 V, V_{DS} = 0	
			-250	nA		150°C
BV_{GSS}	Gate-Source Breakdown Voltage	-25		V	I_G = -1 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-5		V_{DS} = 10 V, I_D = 1 nA	
I_{DSS}	Saturation Drain Current (Note 1)	5	40	mA	V_{DS} = 10 V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance	5000	10,000	μmho	V_{DS} = 10 V, I_D = 5 mA	f = 1 kHz
g_{fs}	Common-Source Forward Transconductance	5000	10,000		V_{DG} = 10 V, I_D = 5 mA	f = 100 MHz
g_{os}	Common-Source Output Conductance		150		V_{DS} = 10 V, I_D = 5 mA	f = 1 kHz
g_{oss}	Common-Source Output Conductance		150		V_{DG} = 10 V, I_D = 5 mA	f = 100 MHz
C_{iss}	Common-Source Input Capacitance		5	pF		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			
$\overline{e_n}$	Equivalent Input Noise Voltage		30	$\frac{nV}{\sqrt{Hz}}$		f = 10 kHz
$\frac{I_{DSS1}}{I_{DSS2}}$	Drain Current Ratio at Zero Gate Voltage (Note 1)	0.85	1		V_{DS} = 10 V, V_{GS} = 0	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		100	mV	V_{DG} = 10 V, I_D = 5 mA	
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio	0.85	1			f = 1 kHz
$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		20	μmho		

NOTE:

1. Pulse test required, pulse width = 300 μs, duty cycle ≤ 30%.

Intersil

N–CHANNEL SILICON J FET

U308 U309 U310 U311

FEATURES

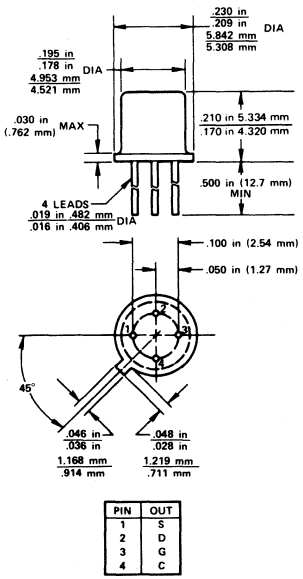
- High Power Gain
  - 15dB Typical at 100MHz, Common Gate
  - 10dB Typical at 450MHz, Common Gate
- Low Single Sideband Noise Figure
  - 1.5dB Typical at 100MHz, Common Gate
  - 3.2dB Typical at 450MHz, Common Gate
- Wide Dynamic Range – Greater than 100dB
- Offered in Wide Variety of Packages for Most Any Circuit Configuration.

GENERAL DESCRIPTION

This family of N-channel Junction FETs are designed and characterized for VHF and UHF applications requiring high gain and low noise figure. The forward transconductance is relatively flat out to 1000MHz. Applications for these devices in military, commercial and consumer communications equipment include low noise, high gain RF amplifiers, low noise mixers with conversion gain, and low noise, ultra stable RF oscillators.

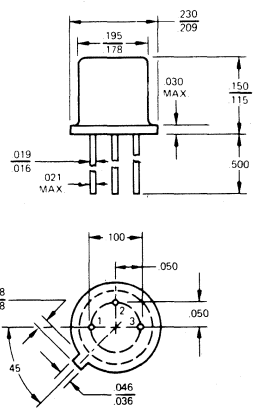
PACKAGE DIMENSIONS

TO-72



PIN	OUT
1	S
2	D
3	G
4	C

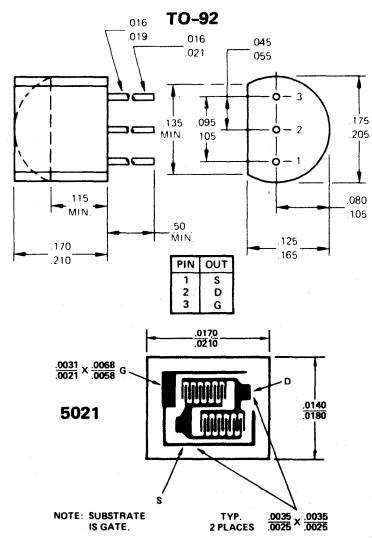
TO-52



Gate is in electrical contact with case

PIN	OUT
1	S
2	D
3	G

TO-92



PIN	OUT
1	S
2	D
3	G

ORDERING INFORMATION

TO52	TO72	TO92	WAFER	CHIP
U308		U308-TO92	U308/W	U308/D
U309		U309-TO92	U309/W	U309/D
U310		U310-TO92	U310/W	U310/D
	U311			

ABSOLUTE MAXIMUM RATINGS (25°C)

	TO-52	TO-72	TO-92
Gate-Drain or Gate-Source Voltage	–25V	–25V	–25V
Gate Current	20mA	10mA	10mA
Total Power Dissipation	500mW	300mW	300mW
Power Derating (to maximum operating temperature)	4.0mW/°C	2.4mW/°C	3.0mW/°C
Operating Temperature Range	–65 to 150°C	–65 to +150°C	–55 to +125°C
Storage Temperature Range	–65 to 200°C	–65 to +200°C	–55 to +125°C
Lead Temperature (1/16" from case for 10 sec)	300°C	300°C	300°C

ELECTRICAL CHARACTERISTICS FOR U308, U309 and U310 (25°C unless otherwise noted)

CHARACTERISTIC		U308			U309			U310			UNIT	TEST CONDITIONS	
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{GSS}	Gate Reverse Current			-150			-150			-150	pA	V_{GS} = -15 V	
				-150			-150			-150	nA	V_{GS} = 0	T = 125°C
BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25			-25			V	I_G = -1 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1.0		-6.0	-1.0		-4.0	-2.5		-6.0	V	V_{DS} = 10 V, I_D = 1 nA	
I_{DSS}	Saturation Drain Current (Note 1)	12		60	12		30	24		60	mA	V_{DS} = 10 V, V_{GS} = 0	
$V_{GS(f)}$	Gate-Source Forward Voltage			1.0			1.0			1.0	V	I_G = 10 mA, V_{DS} = 0	
g_{fg}	Common-Gate Forward Transconductance (Note 1)	10		20	10		20	10		18	mmho	V_{DS} = 10 V, I_D = 10 mA	f = 1 kHz
g_{ogs}	Common-Gate Output Conductance			150			150			150	μmho		
C_{gd}	Drain-Gate Capacitance			2.5			2.5			2.5	pF	V_{GS} = -10 V, V_{DS} = 10 V	f = 1 MHz
C_{gs}	Gate-Source Capacitance			5.0			5.0			5.0			
$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		10			10			10		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10 V, I_D = 10 mA	f = 100 Hz
g_{fg}	Common-Gate Forward Transconductance		12			12			12		mmho	V_{DS} = 10 V, I_D = 10 mA	f = 100 MHz
			11			11			11				f = 450 MHz
g_{ogs}	Common-Gate Output Conductance		0.18			0.18			0.18				f = 100 MHz
			0.7			0.7			0.7				f = 450 MHz
G_{pg}	Common-Gate Power Gain		15			15			15		dB		f = 100 MHz
			10			10			10				f = 450 MHz
NF	Noise Figure		1.5			1.5			1.5				f = 100 MHz
			3.2			3.2			3.2				f = 450 MHz

ELECTRICAL CHARACTERISTICS FOR U311 (25°C unless otherwise noted)

CHARACTERISTIC		U311			TEST CONDITIONS	
		MIN	MAX	UNIT		
I_{GSS}	Gate Reverse Current		-150	pA	V_{GS} = -15V, V_{DS} = 0	
			-150	nA		150°C
BV_{GSS}	Gate-Source Breakdown Voltage	-25		V	I_G = -1 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-6		V_{DS} = 10V, I_D = 1 nA	
I_{DSS}	Saturation Drain Current (Note 1)	20	60	mA	V_{DS} = 10V, V_{GS} = 0	
$V_{GS(f)}$	Gate-Source Forward Voltage		1	V	I_G = 1 mA, V_{DS} = 0	
g_{fg}	Common-Gate Forward Transconductance (Note 1)	10,000	20,000	μmho	V_{DS} = 10V, I_D = 10 mA	f = 1 kHz
g_{ogs}	Common-Gate Output Conductance		150			
C_{gd}	Gate-Drain Capacitance		2.5	pF	V_{DG} = 10V, I_D = 5 mA	f = 1 MHz
C_{gs}	Gate-Source Capacitance		5.0			

NOTE: 1. Pulse test duration = 2 ms

GLOSSARY OF TERMS AND ABBREVIATIONS

FIGURES OF MERIT

Input impedance	$\frac{1}{I_{gss}} + \frac{1}{C_{ISS}}$
Voltage gain	$\frac{g_{fs}}{I_{DS}}$ or $\frac{BV_{DGO}}{V_{GS(OFF)}}$
Frequency cutoff	$\frac{g_{fs}}{C_{rss}}$
Noise figure	$\frac{1}{e_n} + \frac{1}{R_S i_n}$
Distortion	$\frac{V_{GS(OFF)}}{V\ Signal}$
Switching efficiency	$\frac{r_{DS}}{I_{D(OFF)}}$

COMMON DEFINITIONS

FET Term	Definition	Transistor Term
g_{fs}	Small signal forward gain	hfe
BV_{DGO}	Maximum applied voltage	BV_{CEO}
I_{DGO} (I_{GSS})	Input leakage current	I_{CBO}
r_{DS}	On resistance	R SAT (V_{CESAT} Equiv.)
C_{rss}	Output capacitance	C_{ob}
C_{iss}	Input capacitance	C_{ib}
y_{os}	Output admittance	1/hoe

IMPORTANT FET PARAMETER RELATIONSHIPS

$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(OFF)}}\right)^2$	Variation of drain current with gate bias.
$g_{fs} = g_{fso}\left(1 - \frac{V_{GS}}{V_{GS(OFF)}}\right)$	Variation of y_{fs} with gate bias.
$g_{fs} = g_{fso}\sqrt{\frac{I_D}{I_{DSS}}}$	Variation of y_{fs} with drain current.
$V_{GS(OFF)} = \frac{2\ I_{DSS}}{y_{fso}}$	Pinch-off voltage in terms of I_{DSS} and y_{fs}.
$NF_{min} = 10 \log\left(1 + \frac{e_n i_n}{K_T}\right)$	Min noise figure obtainable in ckt. using optimum resistor.
$R_{opt} = \frac{e_n}{i_n}$	Optimum resistance for lowest noise figure in ckt.
$D_H = \frac{25\ e_{in}}{V_{GS(OFF)} - V_{GS}}$	Harmonic Distortion for large signal amplifier.
$V_{GS(OFF)} = 1.45\ V_{GS}$ @ $I_D = 0.1\ I_{DSS}$	Pinch-off voltage in terms of V_G at a drain current of 1/10 I_{DSS}.
$R_{DS} \approx \frac{K\ V_{GS(OFF)}^2}{I_{DSS}(V_{GS(OFF)} - V_{GS})}$ K = 0.4 to 0.9	Variation of drain resistance in the triode region in terms of I_{DSS} and V_P with gate bias.
$R_{DS(on)T} = R_{DS(on)}$ @ 25°C x (1 + .007 T_A)	"ON" Resistance chg as function of temp. Note: Increases as T_A increases.
$f_T = \frac{g_{fs}}{2\pi C_{iss}}$	Bandwidth of FET Device.
$r_{DS} = \frac{r_{DSo}}{1 - \frac{V_{GS}}{V_{GS(OFF)}}}$	"On Resistance" as a function of Gate-Source Voltage. Note: $R_{DS} \approx 1/y_{fs}$

FET APPLICATIONS AND IMPORTANT PARAMETERS

Low-Freq. Amplifier	Electro-meter Amplifier	Low-Noise Amplifier	Low DC Drift Single-Ended Amplifier	High-Freq. Amplifier	Differential Amplifier	Analog Switch	Digital Switch
g_{fs}	I_{GSS}	e_n and i_n	I_{DZ} (I_D zero TC)	g_{fs}	$\lvert V_{GS1} - V_{GS2}\rvert$	$r_{ds(on)}$	$r_{DS(ON)}$
I_{DSS}	g_{fs}	NF	g_{fs} at I_{DZ}	y_{is}	$\frac{\Delta\lvert V_{GS1} - V_{GS2}\rvert}{\Delta T}$	$I_{D(OFF)}$	$r_{ds(on)}$
$V_{GS(OFF)}$	I_{DZ}	g_{fs}	V_{GS} at I_{DZ}	NF	$\lvert I_{G1} - I_{G2}\rvert$	C_{dgs}, C_{sgs}	$V_{GS(OFF)}$
C_{iss}		I_{DSS}	I_G at I_{DZ}	C_{rss}	g_{fs}	C_{rss}	$t_{on} + t_{off}$
C_{rss}		$V_{GS(OFF)}$		I_{DSS}	g_{fs1}/g_{fs2}	$V_{GS(OFF)}$	C_{iss}
				$V_{GS(OFF)}$			
				C_{iss}			

TERMS AND ABBREVIATIONS

TERMS AND SYMBOLS FOR JUNCTION FIELD EFFECT TRANSISTORS

Parameter	Definition	Specified test Conditions
BV_{DGO} (Volts)	Breakdown Voltage (Drain to Gate)	I_G
BV_{GSO} (Volts)	Breakdown Voltage (Gate to Source)	I_G
$V_{(BR)GSS}$ (Volts)	Breakdown Voltage (Gate to Drain and Source)	I_G, $V_{DS} = 0$
C_{DGO} (pF)	Drain to Gate Capacitance	V_{DG}
C_{SGO} (pF)	Gate to Source Capacitance	V_{GS}
C_{iss} (pF)	Total Common-Source Input Capacitance	V_{DS}, V_{GS}
C_{rss} (pF)	Drain to Gate Capacitance under specified conditions	V_{DS}, V_{GS}
$\bar{e}_n$ (nV/$\sqrt{Hz}$)	Equivalent Input Noise Voltage	V_{DS}, I_{DS} or V_{GS}, Freq., BW
G_{fs} (μmhos)	Forward Transconductance at specified operating point	V_{DS}, I_{DS}
g_{fs} (μmhos)	Small Signal Forward Transconductance	V_{DS}, $V_{GS} = 0$
$I_{D(OFF)}$ (nA)	Drain Current with specified Drain Voltage and Gate biased to maximum Vp	V_{DS}, V_{GS}
I_{DGO} (nA)	Drain to Gate Leakage Current	V_{DG}
I_{DSS} (mA)	Zero Bias Drain Current	V_{DS}, $V_{GS} = 0$
I_{GSO} (nA)	Gate to Source Leakage Current	V_{GS}
I_{GSS} (nA)	Total Gate Leakage Current	V_{GS}, $V_{DS} = 0$
I_G (nA)	Gate Leakage Current under specified conditions	V_{DS}, I_{DS}
i_n (pA/$\sqrt{Hz}$)	Equivalent Input Noise Current	V_{DS}, I_{DS} or V_{GS} Freq., BW
CMRR (dB)	Common Mode Rejection Ratio	ΔV_{DG}, I_D ΔV_{GS}

Parameter	Definition	Specified test Conditions
$V_{(BR)G_1G_2}$ (Volts)	Gate to Gate Breakdown Voltage (Monolithic Construction)	V_{DS}, V_{GS}, I_D
$V_{GS(OFF)}$ (Volts)	Gate Source Cut-off Voltage — Gate biased to reduce I_D to specified low level	V_{DS}, I_D
V_{GS} (Volts)	Gate Source Voltage at Operating Point	V_{DG}, I_D
r_{ds} (ohms)	Drain to Source Bulk Resistance	V_{DS}, I_D, f
$r_{DS(ON)}$ (ohms)	On Resistance — Zero Gate Bias	V_{DS} or I_D, $V_{GS} = 0$
Y_{is} (g_{is}) (μmhos)	Common Source Input Capacitance	V_{DS}, I_D
Y_{os} (g_{os}) (μmhos)	Common Source Output Admittance	V_{DS}, I_D
NF (dB)	Noise Figure under specified conditions	V_{DS}, I_{DS} or V_{GS}, R_G Freq., BW
G_{PS} (dB)	Power Gain	V_{DS}, I_D
t_d (nsec)	Delay Time	Specified Test Circuit
t_r (nsec)	Rise Time	Specified Test Circuit
$t_{(off)}$ (nesc)	Turn Off Time	Specified Test Circuit
t_{on} (nesc)	Turn On Time	Specified Test Circuit
t_f (nsec)	Fall Time	Specified Test Circuit

MATCHING CHARACTERISTICS

I_{DSS1}/I_{DSS2} (ratio)	Zero Gate Voltage— Drain Current Ratio	V_{DS}
g_{fs1}/g_{fs2} (ratio)	Transconductance Ratio	V_{DG}, I_D
$\lvert V_{GS1} - V_{GS2} \rvert$ (mV)	Gate-Source Differential Voltage	V_{DG}, I_D
$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$ (μV/°C)	Voltage Change due to a change in temperature	T_A, V_{DG}, I_D
$\lvert I_{G1} - I_{G2} \rvert$ (nA)	$Gate_1$ to $Gate_2$ Leakage Current Differential	V_{DG}, I_D

TERMS AND ABBREVIATIONS

TERMS AND SYMBOLS FOR TRANSISTORS

BV_{CBO} — **Collector-Base Breakdown Voltage with Emitter Open-Circuited**

The breakdown voltage of the collector-base junction, measured at a specified current, with the emitter open-circuited.

BV_{CEO} — **Collector-Emitter Breakdown Voltage with the Base Open-Circuited**

The collector-emitter breakdown voltage, measured at a specified collector current, with the base open-circuited.

BV_{CER} — **Collector-Emitter Breakdown Voltage with Resistance between Emitter and Base**

The collector-emitter breakdown voltage measured at a specified current with a specified resistance R connected between the base and the emitter.

BV_{CES} — **Collector-Emitter Breakdown Voltage with Base Shorted to Emitter**

The collector-emitter breakdown, measured at a specified current, with the base shorted to the emitter.

BV_{CEX} — **Collector-Emitter Breakdown Voltage at a Specified Condition**

The collector-emitter breakdown voltage measured at a specified current with the base-emitter junction forward or reverse biased by a specified voltage or current.

BV_{EBO} — **Emitter-Base Breakdown Voltage with Collector Open-Circuited**

The emitter-base breakdown voltage, measured at a specified current, with the collector open-circuited.

h_{FE} — **Common-Emitter DC Current Gain**

The ratio of DC collector current to DC base current measured at a specified collector-emitter voltage and a specified collector current.

I_{CBO} — **Inverse Collector-Base Current**

The collector-base current with the junction reverse biased by a specified voltage, with the emitter open-circuited.

I_{CEX} — **Inverse Collector-Emitter Current at a Specified Condition**

The collector-emitter current measured at a specified collector-emitter voltage with the base forward or reverse biased by a specified voltage or current.

I_{EBO} — **Inverse Emitter-Base Current**

The emitter-base current with the junction reverse biased by a specified voltage with the collector open-circuited.

LV_{CEO}, LV_{CER}, LV_{CES}, LV_{CEX}, or, V_{CEO} (sust) V_{CER} (sust) V_{CES} (sust) V_{CEX} (sust) — **Pulsed Limiting Breakdown Voltages**

These are similar to the corresponding, above defined, BV parameters but are measured at a specified high current point where collector-emitter voltage is lowest. The duration of the pulse and its duty cycle must be specified. The letter L indicates LIMITING Value and is measured outside the negative resistance zone of the reverse characteristic.

$V_{BE(ON)}$ — **Unsaturated Base-Emitter Voltage**

The base-emitter voltage measured in the common-emitter connection at a specified collector to emitter voltage and specified collector current.

$V_{BE(SAT)}$ — **Base-Emitter Saturation Voltage**

The base-emitter voltage measured in the common-emitter connection at a specified collector and base saturation currents.

$V_{CE(SAT)}$ — **Collector-Emitter Saturation Voltage**

The collector-emitter voltage measured in the common-emitter connection at specified collector and base saturation currents.

V_{RT} — **Reach Through Voltage**

V_{PT} — **Punch Through Voltage**

The collector-base voltage above which an increase of applied voltage can be measured in the emitter-base open circuit.

C_{ob} — **Common-Base Output Capacitance**

The common-base output capacitance with input ac open.

TERMS AND ABBREVIATIONS

TERMS AND SYMBOLS FOR TRANSISTORS

C_{re}	**Common Emitter Reverse Transfer Capacitance** This parameter is the imaginary part of y_{re}. When $I_C = 0$, C_{re} is identical to C_{CB}.
C_{TE}	**Base-Emitter Capacitance** The capacity of the base-emitter junction at a specified inverse voltage with the collector open.
C_{CB}	**Collector Base Capacitance** Collector Base Capacitance measured at some Specified Collector Base Voltage.
CG_e, CG_b	**Conversion Gain, Common-Emitter or Common-Base** The ratio of the output power of a mixer, at one specified frequency, to its input power, at another specified frequency. This parameter is a function of oscillator injection voltage and the mixer operating point.
$f_{\alpha b}$, $f_{h_{fb}}$	**Common-Base Cut Off Frequency** The frequency at which the h_{fb} (α) is reduced to 0.707 of its low frequency value.
f_β, $f_{h_{fe}}$	**Common-Emitter Cut Off Frequency** The frequency at which the h_{fe} (β) is reduced to 0.707 of its low frequency value.
	Gain Band-Width Product The common-emitter current gain band-width product in the frequency range where the current gain is falling at approximately 6 dB/octave.
f_t	**Maximum Frequency of Oscillation** This parameter is a device figure of merit that is calculated from ft and rb'Cc.
G_C	**Common-Emitter Power Gain**
G_{TE}	**Common Emitter Transducer Gain** A test fixture must be specified.
GMA	**Stability Limited Gain or Gain Maximum Available** This parameter is a device figure of merit and must be calculated from the two port "y" parameters.
h_{fe}	**Common-Emitter Current Gain** The common-emitter forward current transfer ratio with output ac shorted. This is a complex quantity.
h_{ie}	**Common-Emitter Input Impedance** The common-emitter input impedance with the output ac shorted. This is a complex quantity.
h_{oe}	**Common-Emitter Output Admittance** The common-emitter output admittance with the input ac open. This is a complex quantity.
h_{re}	**Common-Emitter Reverse Voltage Transfer Ratio** The common-emitter reverse voltage transfer ratio with input ac open. This is a complex quantity.
MAG	**Maximum Available Gain** Device figure of merit that must be calculated from the two port "y" parameters.
MSG	**Maximum Stable Gain** This parameter is a device figure of merit that is calculated from the two port "y" parameters.
NF	**Noise Figure** Noise figure = 10 $\log_{10}$F, where F is the ratio of total output noise power to the output power due solely to the thermal noise of the source impedance.
r_{bb}', r_b'	**Base <<Spreading>> Resistance** Equivalent to the real part of h_{ie} at some specified very high frequency.

TERMS AND ABBREVIATIONS

TERMS AND SYMBOLS FOR TRANSISTORS

$rb'C_c$ — Collector Base Time Constant

This parameter is a device figure of merit and is measured in a specified test circuit.

Common-Emitter Switching Parameters

In the following, drive circuit conditions and collector circuit conditions must be specified. The transition times of the input must be negligible compared to the measured times.

t_d — Delay Time

The time interval during turn-on from the point when the input pulse at the base reaches 10% of its full amplitude to the point when the collector pulse changes from 0 to 10% of its maximum amplitude.

t_r — Rise Time

The time interval during turn-on in which the collector pulse changes from 10% to 90% of its maximum amplitude.

t_s — Storage Time

The time interval during turn-off from the point when the turn-off pulse at the base changes from 100% to 90% of its full amplitude to the time when the collector current has changed from 100% to 90% of its maximum amplitude.

t_f — Fall Time

The time interval during turn-off in which the collector pulse decreases from 90% to 10% of its maximum amplitude.

R_{TH} — Internal Junction-to-Case Thermal Resistance

The rated increase of junction temperature with respect to the case temperature per unit of dissipated power. It is also called Thermal Resistance with infinite heat sink.

θ_{JC} — Junction-to-Case Thermal Rating

θ_{JA} — Junction-to-Ambient Thermal Rating

$\frac{h_{FE1}}{h_{FE2}}$ — DC Current Gain or Beta Ratio

y_{fe} — Common-Emitter Forward Transfer Admittance

The common-emitter forward transfer admittance with output ac shorted. This is a complex quantity ($g_{fe} + jb_{fe}$).

y_{ie} — Common-Emitter Input Admittance

The common-emitter input admittance with output ac shorted. This is a complex quantity ($g_{ie} + b_{ie}$).

y_{oe} — Common-Emitter Output Admittance

The common-emitter output admittance with input ac open. This is a complex quantity ($g_{oe} + jb_{oe}$).

y_{re} — Common-Emitter Reverse Transfer Admittance

The common-emitter reverse transfer admittance with input ac shorted. This is a complex quantity ($g_{re} + jb_{re}$).

η — Collector Efficiency

This parameter applies to oscillators and class C amplifiers, predominantly. It is defined as the ratio of RF Power Out/DC Power In.

P_o — Power Out

This parameter applies to oscillators. The units are watts and a test circuit must be specified.

$V_{BE1} - V_{BE2}$ — Differential Match between Emitter and Base Voltages or $V_{BE(ON)}$ Voltages

$\frac{\Delta(V_{BE1} - V_{BE2})}{\Delta T}$ — Differential Emitter-Base Voltage Change with Temperature

$I_{B1} - I_{B2}$ — Differential Base Current Draw

$\frac{\Delta(I_{B1} - I_{B2})}{\Delta T}$ — Differential Base Current Draw with Temperature

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